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Seungju Yoon,[1] Hyun Jae Lee,[2] and Taehwan Moon[1,3,a)]

AFFILIATIONS

[1]Department of Electrical and Computer Engineering, Ajou University, Suwon, Gyeonggi, South Korea
[2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA
[3]Department of Intelligence Semiconductor Engineering, Ajou University, Suwon, Gyeonggi, South Korea

[a)]Author to whom correspondence should be addressed: taehwanm@ajou.ac.kr

ABSTRACT

Two-dimensional electron gases (2DEGs) at epitaxial oxide interfaces, such as $LaAlO_3/SrTiO_3$ heterostructures, have long served as model platforms for exploring emergent interfacial phenomena, including superconductivity, magnetism, and tunable metal–insulator transitions. While such systems were initially investigated primarily within the context of condensed matter physics, their relevance is being redefined by recent advances in non-epitaxial oxide 2DEGs, which offer new opportunities for practical applications. In contrast to polarity-driven epitaxial interfaces, non-epitaxial oxide 2DEGs are often governed by chemically driven carrier generation mechanisms, most notably oxygen vacancy (V_O) formation induced by interfacial redox reactions. These mechanisms enable systematic tuning of interfacial electronic properties using amorphous or polycrystalline oxides and industry-compatible processes. This review provides a unified perspective linking the fundamental formation mechanisms of oxide 2DEG to their emerging applications. We first survey the principal physical origins of oxide 2DEGs, followed by an in-depth discussion of V_O generation pathways in non-epitaxial oxide systems, including ionic bombardment, metal-induced redox reactions, and surface chemical effects. Building on this mechanistic foundation, we connect interfacial chemistry to application-level performance metrics, with particular emphasis on memory and neuromorphic technologies motivated by rapidly expanding computational demands in the AI era. In memory architectures, oxide 2DEGs are evaluated as enablers of both selector devices and storage elements, while in neuromorphic hardware, sensor platforms exploiting 2DEG transport are highlighted for their capability to emulate biological sensory functions and dynamics. Key challenges for practical deployment of oxide 2DEGs, including compatibility with three-dimensional integration, thermal stability during processing, and limitations in material selection, are critically examined. Potential strategies for overcoming these constraints, such as interfacial chemistry control, defect engineering, and process–structure–property correlations, are discussed. By bridging the fundamental physics and chemistry of oxide 2DEGs with emerging device-level applications, this review underscores their potential as a cornerstone material platform for next-generation, energy-efficient computing architectures.

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I. INTRODUCTION

Two-dimensional electron gases (2DEGs) represent a foundational concept in condensed matter physics and electronic device engineering. By confining free carriers to motion in a two-dimensional plane, typically at the interface between two distinct materials, 2DEGs exhibit unique electronic behaviors that are markedly different from those of their three-dimensional (3D) counterparts. Unlike bulk electron systems, where carrier motion is delocalized in all directions, electrons in a 2DEG are quantized in the direction perpendicular to the plane, resulting in discrete subband levels, reduced scattering phase space, and enhanced carrier mobility. This reduced dimensionality has enabled the emergence of exotic quantum phenomena such as the integer and fractional quantum Hall effects, quantum interference, and strong spin–orbit coupling effects, which are otherwise difficult to observe in bulk systems.

Historically, high-mobility 2DEGs were first realized in III–V semiconductor heterostructures such as AlGaAs/GaAs through modulation doping,[1–3] which established the basis of interfacial carrier confinement enabled by band alignment and internal electric field. These high electron mobility transistor (HEMT) systems demonstrated how electrostatic design at heterointerfaces can produce highly mobile electron layers with reduced impurity scattering. Building on this conceptual framework, subsequent studies have shown that 2DEG can also arise from a broader range of physical and chemical mechanisms, particularly in complex oxide heterostructures.

More generally, 2DEGs can arise from a variety of physical mechanisms, including electrostatic potential gradients across heterointerfaces, bandgap discontinuities, internal dipoles, polar discontinuities, and defect-induced charge transfer.[4–7] At oxide interfaces in particular, these mechanisms can coexist or compete, rendering the resulting electron layer highly sensitive to interfacial chemistry, defect structure and processing conditions. This sensitivity not only governs carrier confinement and scattering but also enables active control of electronic properties through external gating or chemical modification, positioning oxide-based 2DEGs as a versatile platform for both fundamental studies and functional device applications.

Building on these principles, the discovery of 2DEGs at oxide interfaces, most notably in perovskite-based heterostructures such as $LaAlO_3/SrTiO_3$ (LAO/STO) heterointerface, has sparked immense interest in condensed matter physics and oxide electronics. Initially regarded as a quantum playground for exploring interface-driven phenomena including superconductivity, magnetism, and Rashba spin splitting,[8–13] oxide 2DEGs have evolved into a platform with rich fundamental physics and compelling technological promise. Confined within a few nanometers of the heterointerfaces, these electron systems exhibit high mobility, gate tunability, and versatile electrostatic control, making them attractive for next-generation electronic devices.

In early studies, the origin of interfacial conductivity in oxide heterostructures was attributed to several mechanisms, including electronic reconstruction due to polar discontinuity, oxygen vacancy (V_O) formation, and cation intermixing.[14–17] Among these, polar-catastrophe-driven charge transfer and oxygen stoichiometry effects played central roles in shaping early theoretical and experimental understanding of carrier generation at oxide interfaces. As insight into these underlying principles matured, research direction gradually shifted toward identifying routes to realize practical, stable, and scalable 2DEG platforms beyond epitaxial systems.

One major enabler of this transition has been the ability to deliberately manipulate V_O at interfaces. The charge transfer mechanism often discussed in epitaxial LAO/STO systems has been attributed to polar discontinuity, although alternative contributions have also been reported. Such mechanisms typically require epitaxially grown, atomically abrupt polar films and therefore constrain the material selection and fabrication flexibility. In contrast, V_O-mediated mechanisms have proven to be far more versatile: 2DEG formation driven by V_O has been demonstrated not only in epitaxial heterostructures but also in amorphous and polycrystalline oxide systems, significantly broadening the scope of compatible material systems and deposition methods.

To this end, various strategies for generating V_O, including ionic bombardment, metal-induced redox reactions, and surface chemical reactions, have broadened the accessible material and process window for 2DEG formation. In particular, the adoption of atomic layer deposition (ALD), a technique that operates under relatively low vacuum and moderate temperatures, offers substantial advantages over conventional high-vacuum epitaxial methods such as pulsed laser deposition (PLD). Unlike PLD, which typically requires high vacuum conditions and high substrate temperatures, ALD enables conformal coating with sub-nanometer thickness control, excellent film uniformity, and precise interface engineering on 3D structures. Furthermore, ALD is inherently scalable and CMOS-compatible, and is widely employed in modern semiconductor manufacturing for various functional layers. These merits have opened new routes for integrating 2DEG functionalities onto CMOS-compatible substrates and vertically stacked device architectures, pushing 2DEG research beyond fundamental exploration into the realm of practical oxide electronics.

These advancements have catalyzed a shift from purely physics-driven investigations toward application-oriented research, where 2DEG-based systems are actively explored for functional electronic devices (Fig. 1). Although functional devices and even circuits had already been demonstrated in epitaxial oxide 2DEG systems, recent progress in chemically induced and low-temperature-processed oxide interfaces has substantially broadened the accessible materials space and strengthened the prospects for scalable device integration.[18,19] Recent studies have demonstrated their potential in field-effect transistors (FET), resistive switching memories (RRAM), neuromorphic synapses, and threshold switching selectors. The intrinsic tunability, nonvolatility, and strong interfacial confinement of 2DEGs render them promising building blocks for highly dense, energy-efficient, and adaptive electronic systems.

In this review, we comprehensively examine recent advances in the formation and utilization of 2DEGs at oxide interfaces, with particular emphasis on the evolution from fundamental mechanisms to

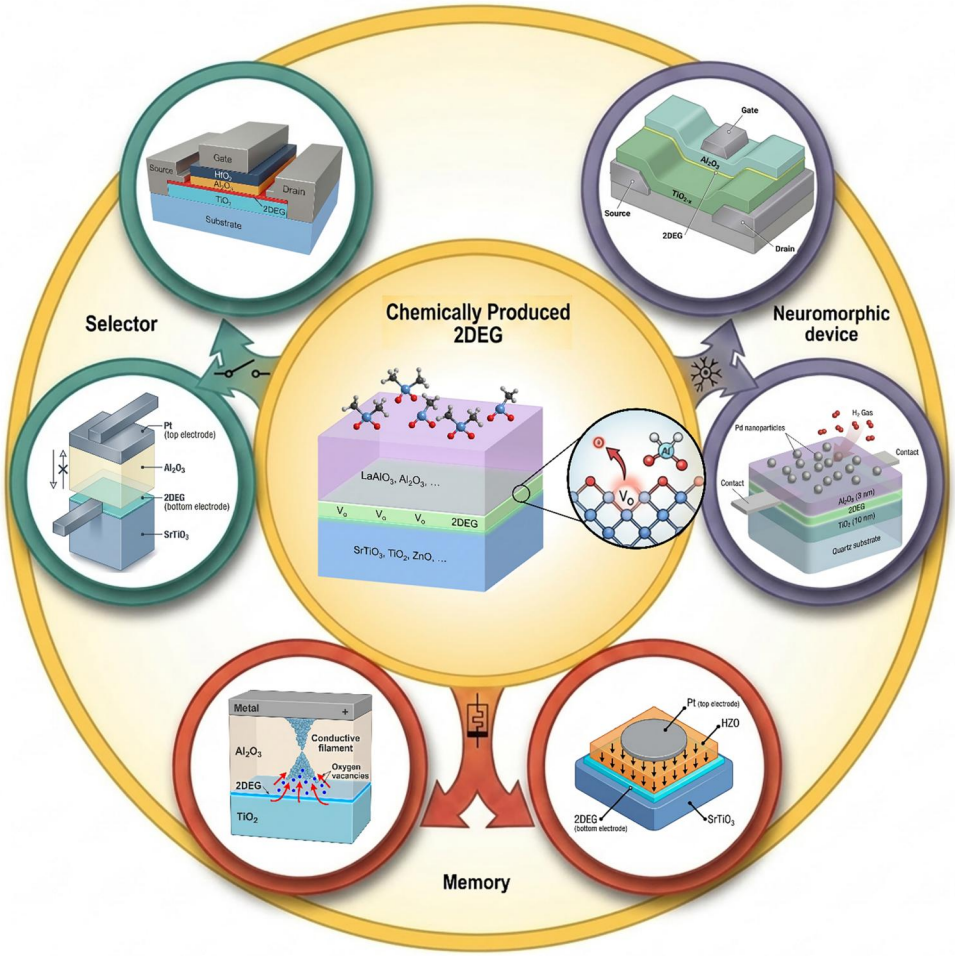

FIG. 1. Chemically produced oxide 2DEG and device applications. This single-panel schematic illustrates an oxide 2DEG formed at oxide heterointerfaces through oxygen-vacancy-driven interfacial redox reactions. The resulting interface-defined conductive channel or electrode provides a common materials platform for representative device applications, including selector devices, memory elements, and neuromorphic/sensory devices.

application-ready architectures. We first outline the physical origins and classification of 2DEG formation routes in oxides, including canonical mechanisms such as polar discontinuity-driven electronic reconstruction, V_O–mediated doping, and emerging redox-free charge transfer pathways. These mechanisms are discussed in the context of both epitaxial and amorphous material systems.

We then focus on engineering strategies for V_O manipulation and interfacial chemical reactions, which have proven central to achieving 2DEG formation under scalable and CMOS-compatible conditions. Approaches such as ALD ligand chemistry, photoinduced surface reactions, and thermodynamically driven oxygen exchange are examined and classified based on their mechanistic origins, including metal-induced redox, and ligand-driven reduction. This framework establishes a direct link between material chemistry and electronic structure control.

Building on these materials-level considerations, we review progress in translating oxide 2DEG functionalities into electronic components, including nonvolatile resistive memories (RRAM), threshold switching selectors, and neuromorphic devices. Particular attention is given to demonstrations of energy-efficient, gate-tunable, and multistate operation enabled by confined electron channels, as well as emerging efforts toward 3D integration and vertical device stacking using amorphous or low-temperature-processed oxide layers.

Finally, we discuss remaining challenges and future directions for scalable 2DEG integration in functional electronics. Perspectives are offered on interface-engineered heterostructures and hybrid material stacks that combine 2DEG conduction with additional functionalities such as ferroelectricity, ionic motion, or phase change behavior. By bridging fundamental principles with device-level implementations, this review aims to serve as a comprehensive resource for both understanding oxide 2DEG physics and guiding their deployment in emerging memory, logic, and neuromorphic technologies.

II. PRINCIPLES OF 2DEG AT OXIDE INTERFACES

The formation of 2DEG at oxide interfaces arises from a diverse set of physical and chemical mechanisms that redistribute charge across heterointerfaces. Unlike conventional semiconductor heterostructures, oxide systems exhibit strong coupling between electrostatics, lattice polarization, defect chemistry, and electronic correlations, allowing multiple compensation pathways to coexist or compete. Understanding these underlying principles is therefore essential for

distinguishing idealized formation limits from mechanisms that dominate under realistic growth and processing conditions.

In this section, we examine the fundamental mechanisms that govern 2DEG formation at oxide interfaces. We begin with the polar-catastrophe framework, which represents an ideal electrostatic limit for charge reconstruction at polar/nonpolar heterointerfaces. We then discuss V_O-mediated charge donation as a chemically driven compensation pathway that becomes increasingly prominent under non-ideal or scalable processing conditions. Finally, we consider additional mechanisms, such as field-driven ionic migration, cation intermixing, and lattice distortions, that further enrich the parameter space for interfacial charge control. Together, these principles provide a unified foundation for the engineering strategies discussed in subsequent sections.

A. Polar-catastrophe

The polar-catastrophe framework was the first internally consistent mechanism proposed to account for the emergence of interfacial conductivity at polar/non-polar oxide heterointerfaces, most notably LAO/STO. In the ionic limit, LAO consists of alternating $(LaO)^+$/$(AlO_2)^-$ planes stacked along the [001] direction, whereas STO is composed of charge-neutral layers. When a polar LAO film is grown on nonpolar STO, this charge mismatch generates a built-in electric field within the LAO overlayer. If uncompensated, the electrostatic potential would increase linearly with LAO thickness, leading to a divergence commonly referred to as the "polar catastrophe."

The seminal work by Ohtomo and Hwang provided early experimental support for this picture by demonstrating polarity-selective conductivity in LAO/(001)-oriented STO heterostructures with TiO_2 (TO)-terminated STO substrates:[14] metallic behavior at the n-type (LaO/TO) interface and insulating behavior at the p-type (AlO_2/SrO) interface, with the latter rarely exhibiting conductive behavior in practice [Fig. 2(a)].[14] This asymmetry directly links interfacial conduction to the sign of the polar discontinuity, establishing polar mismatch as a driving force for electronic reconstruction at oxide interfaces. Subsequent studies revealed a critical thickness behavior, wherein conduction in well-oxidized LAO/STO heterostructures emerges only when the LAO overlayer exceeds approximately four unit cells.[15] This threshold is consistent with a thickness-dependent potential build-up and band alignment that triggers charge transfer to the interface.

Importantly, this electrostatic scenario represents an idealized limiting case in which electronic reconstruction serves as the primary mechanism for compensating the polar field. One of the most direct experimental validations of this picture comes from systematic dilution of formal polarization. In $(LaO)_x(STO)_{1-x}$ ("Lastex") solid solutions as a top layer, reducing the formal polarization shifts the threshold thickness in proportional to x^{-1}, in agreement with polar-catastrophe expectations [Fig. 2(b)].[20] Careful control of film stoichiometry further reveals that the compensation pathway, whether electronic or atomic, is sensitively governed by interfacial chemistry: stoichiometric or La-rich film can remain insulating, whereas slightly Al-rich film exhibits interfacial conduction.[21]

Spatially resolved transport measurements provide additional constraints on the applicability of the polar-catastrophe limit. Cross-sectional conductive atomic force microscopy (CT-AFM) distinguishes a nanometer-scale interfacial 2DEG in well-oxidized samples from extended, bulk-like conduction associated with V_O doping in low oxygen pressure or non-annealed films.[22] These observations delineate the boundary between electrostatically driven interfacial reconstruction and extrinsic, defect-mediated conduction.

Microscopically, the polar-catastrophe scenario can be understood in terms of band alignment across the heterointerface. As the LAO thickness increases, the potential drop across the polar layer raises the LAO O-2p valence band maximum toward the STO Ti-3d conduction band minimum at the interface. Below the critical thickness, partial screening by polar lattice distortions preserves an insulating state. Once the gap closes, an electronic reconstruction transfers ≈0.5 electrons per interfacial unit cell into Ti-3d states, neutralizing the polar field and forming a 2DEG2324 [Fig. 2(c)]. X-ray linear dichroism further reveals concomitant orbital reconstruction within the Ti-t_{2g} manifold, with the d_{xy} orbital forming the lowest-energy conduction subband and dominating interfacial transport.[25]

B. Oxygen-vacancy

Alongside the electrostatic polar-catastrophe limit, early studies of LAO/STO heterostructures already pointed to an alternative, chemically driven route to interfacial conduction mediated by V_O. V_O created during film growth or post-processing acts as donor defects that supply electrons to Ti-3 *d* states in STO, yielding a high-mobility electron system irrespective of the overlayer's formal polarity. Systematic growth and annealing experiments established a strong correlation between interfacial conductivity and oxygen chemical potential: interfaces grown under low oxygen partial pressure are consistently conducting, whereas higher oxygen pressure (p_{O2}) growth or post-oxidation treatments strongly suppresses carriers, directly implicating V_O donors in STO as the source of the 2DEG.[14,26,27]

Multiple experimental probes reinforce this picture by tying transport properties to oxygen deficiency in STO. Optical signatures characteristic of reduced STO, including blue cathodo/photoluminescence features, emerge in samples grown at oxygen-deficient condition and are reversibly quenched upon re-oxidation [Fig. 3(a)]. Correspondingly, low-temperature (∼10 K) mobilities reaching $\sim 10^4\ cm^2\ V^{-1}\ s^{-1}$, comparable to those of chemically reduced or doped STO, are routinely observed.[23,24] Spectroscopy and ellipsometry studies further reveal Ti^{3+} features whose intensity tracks grown oxygen pressure, while post-annealing in oxygen drives sheet carrier density downward toward an intrinsic upper bound while leaving mobility largely intact [Fig. 3(b)]. This behavior is consistent with donor defects located spatially away from the peak-mobility region.[28]

At the microscopic level, each V_O donates two electrons: $O_O \rightleftharpoons V_O^{2+} + 2e^-$.[29] In the LAO/STO electrostatic landscape, theoretical studies predict a pronounced asymmetry: while the formation energy of V_O is lowest near the p-type (SrO/AlO) side, the donated electrons relax to the n-type (LaO/TiO) interface, where Ti-t_{2g} states (with a lowest d_{xy} subband) host the mobile carriers. This picture naturally explains why n-type interfaces are conducting and p-type ones are insulating, while also reconciling high mobility with V_O-doping via spatial separation between donors and the 2D channel, reminiscent of a modulation-doping-like effect [Fig. 3(c)].[30]

The generality of the V_O-mediated pathway became increasingly clear as interfacial conduction was demonstrated beyond polar perovskite caps. In the spinel/perovskite γ-AO (GAO)/STO system, a high mobility 2DEG emerges despite the absence of a formal polar discontinuity. Conduction onsets above a ∼2 unit-cell GAO threshold

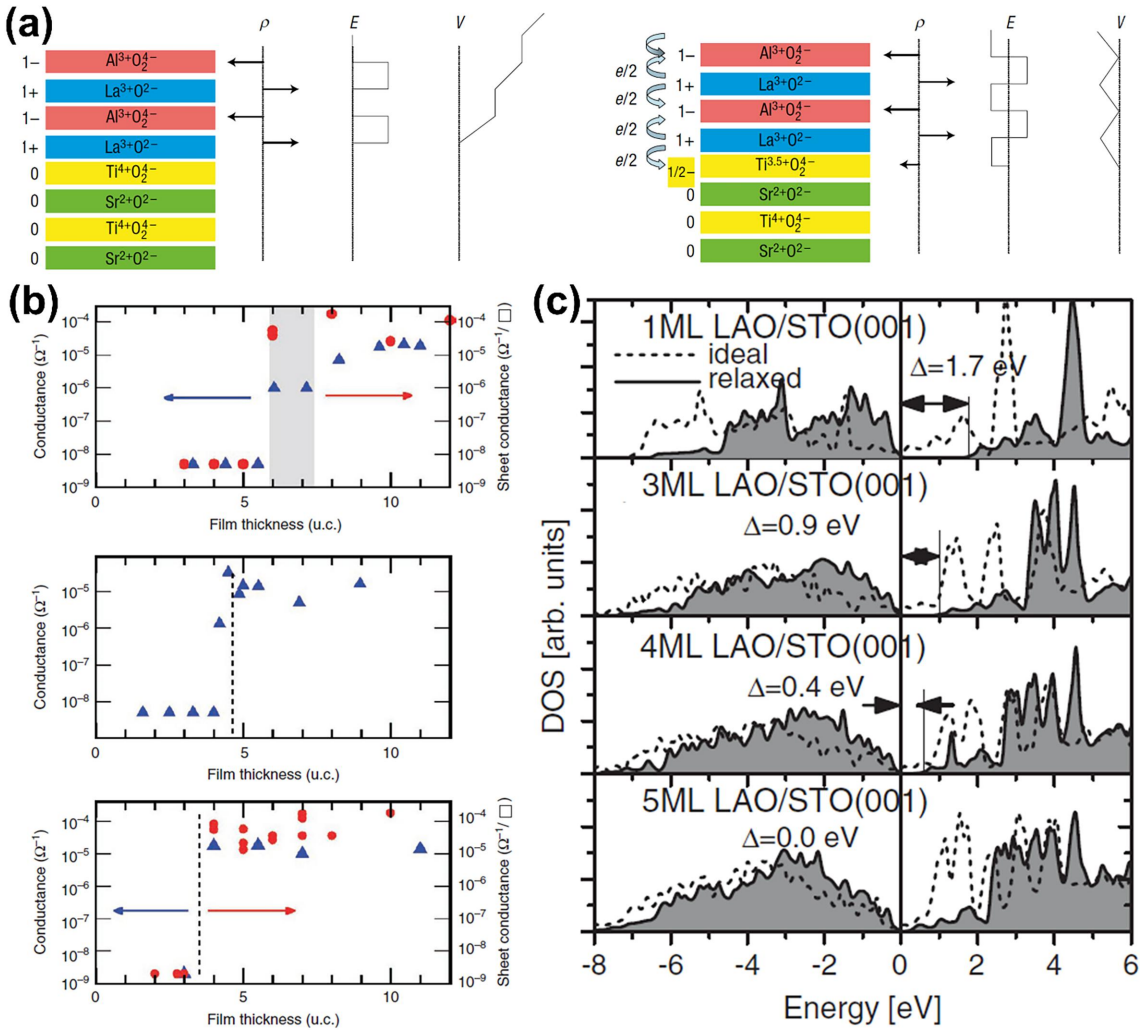

FIG. 2. Atomic-scale origin of polar-discontinuity-driven conduction at LAO/STO interfaces. (a) Schematic illustration of the polar discontinuity at atomically abrupt LAO/(001) STO interfaces, highlighting the electronic reconstruction at the n-type (LaO/TO) interface. Adapted with permission from Nakagawa *et al.*, Nat. Mater. **5**, 204–209 (2006). Copyright 2006 Nature Publishing Group. (b) Room temperature conductance as a function of overlayer thickness for LAO-STO mixed films with different compositions. From top to bottom, the curves correspond to LAO:STO ratios of 0.5:0.5, 0.75:0.25, and 1:0 (pure LAO), respectively. As formal polarization is reduced, the critical thickness for the onset of conductivity increases, in agreement with the intrinsic polar-catastrophe scenario. Adapted with permission from Reinle-Schmitt *et al.*, Nat. Commun. **3**, 932 (2012). Copyright 2012 Macmillan Publishers Limited. (c) First-principles density-of-states calculations show that polar lattice relaxation stabilizes an insulating state for thin LAO films by opening an energy gap, while increasing thickness progressively suppresses this gap, signaling a crossover toward electronic reconstruction. Adapted with permission from R. Pentcheva and W. E. Pickett, Phys. Rev. Lett. **102**, 107602 (2009). Copyright 2009 American Physical Society.

exhibit clear 2D quantum-oscillation signatures and reaches high mobilities ($>10^3$ cm^2 V^{-1} s^{-1} at 10 K), highlighting that a polar catastrophe is not a prerequisite for 2DEG formation when V_O generation is operative.[16,31]

Subsequent work further relaxed structural constraints by demonstrating that long-range crystallinity is not required. Amorphous overlayers deposited on STO can likewise induce interfacial conduction through V_O formation. In amorphous LAO/STO heterostructures, carrier density scales with growth oxygen pressure and is quenched by post-oxidation, accompanied by a corresponding decay of interfacial Ti^{3+} signals.[32,33] This transition marks a significant milestone: the realization of interfacial 2DEG formation using amorphous oxides without relying on epitaxial growth, and more importantly, its implementation via scalable and industry-compatible techniques such as ALD. ALD-based approaches employing amorphous oxides (e.g., *a*-AO and *a*-$YAlO_3$) leverage surface redox reactions to generate V_O at the interface, yielding confined 2DEG with chemistry-set critical thickness on the few-nanometer scale. Angle-resolved x-ray photoelectron spectroscopy (ARXPS) confirms the interfacial localization of reduced Ti species, while side-by-side comparisons with crystalline, oxygen-annealed LAO/STO unambiguously separate V_O-mediated conduction from polar catastrophe driven behavior.[34]

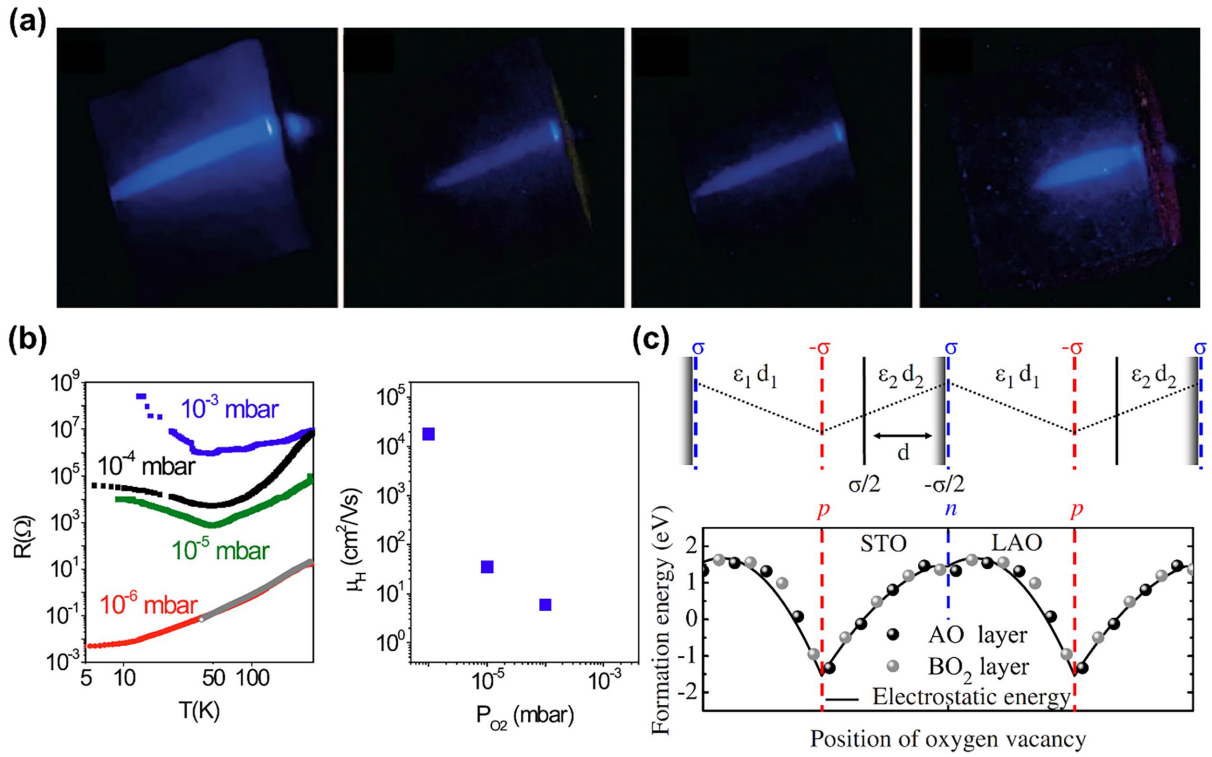

FIG. 3. V_O-driven control of interfacial conduction in LAO/STO heterostructures. (a) Cathodoluminescence images of LAO/STO interfaces subjected to different post-growth treatments show systematic suppression and recovery of luminescence intensity, directly evidencing the reversible annihilation and regeneration of V_O in the STO substrate. Adapted with permission from Kalabukhov *et al.*, Phys. Rev. B **75**, 121404 (2007). Copyright 2007 American Physical Society. (b) Temperature-dependent sheet resistance and low-temperature Hall mobility (measured at 4 K) for interfaces grown under different oxygen partial pressures demonstrate that reduced oxygen pressure during deposition stabilizes a metallic interfacial state with enhanced mobility, consistent with increased V_O concentration. Adapted with permission from G. Herranz *et al.*, Phys. Rev. Lett. **98**, 216803 (2007). Copyright 2007 American Physical Society. (c) First-principles calculations of V_O formation energy across a polar LAO/STO stack reveal that V_Os are energetically favored near the p-type interface, while the electrons released by V_O formation preferentially accumulate at the n-type TO interface, in agreement with an electrostatic capacitor model. Adapted with permission from Z. Zhong *et al.*, Phys. Rev. B **82**, 165127 (2010). Copyright 2010 American Physical Society.

The V_O paradigm extends even further when the single-crystalline STO substrate is replaced altogether. Interfacial conduction has been realized using polycrystalline or amorphous transition-metal oxides such as TO, In_2O_3 (IO), and ZnO as the electron-hosting layer, often grown by ALD on SiO_2/Si substrates. In ALD-fabricated amorphous oxide/TO stacks, a quasi-2DEG emerges once the overlayer exceeds a few nanometers, with sheet carrier densities on the order of 10^{13} –10^{14} cm^{-2} and nanometer-scale confinement.[35] *In situ* cycle-by-cycle resistance tracking and spectroscopy analysis pinpoint the origin to surface chemical reduction of TO during metal-organic precursor (e.g., TMA) pulses, which create V_O donors that populate Ti-3d states. Importantly, improving the crystallinity of TO layer reduces the total V_O density while simultaneously lowering donor activation energies to tens of meV, thereby raising the room-temperature free-carrier density and enhancing 2D confinement.[36,37]

Device-level demonstrations on these thin-film heterostructures underscore the practical implications of V_O-mediated 2DEGs. Top-gated field-effect transistors (FET) fabricated on amorphous-oxide/TO platforms exhibit high on/off ratios exceeding 10^7 and sub-100 mV/dec subthreshold swing when the bottom TO is ultrathin and fully depleted in the off-state.[35] Analogous behavior has been observed at AO/IO interfaces, where short-range-ordered 2DEG-like sheet forms after ALD, again consistent with redox-driven V_O donors; transport and spectroscopic analyses indicate that the 2DEG density and mobility are tunable by the IO microstructure (grain size/ordering) and overlayer chemistry.[38] Together, this V_O-centric paradigm generalizes the 2DEG concept beyond polar discontinuities to polycrystalline and non-perovskite platforms compatible with back-end processing temperature, offering practical routes to selectors, memories, and neuromorphic elements discussed later.

C. Compositional rearrangement

Compositional rearrangements at the interface provide another route to modulating interfacial charge density. Intermixing of A- and B-site cations at polar/non-polar interfaces is primarily driven by concentration gradients, as described by diffusion (Fick's law), and is therefore generally expected between dissimilar materials. Such intermixing influences the polar mismatch and modifies the interfacial electronic structure. Depth-resolved medium-energy ion scattering (MEIS) and STEM-EELS show that conducting 5-u.c. LAO overlayers exhibit a broader La/Sr intermixing region than insulating 3-u.c. films,

indicating that partial cation substitution contributes to donor formation and interfacial doping in STO region [Fig. 4(b)].[39] Cohehert-potential-approximation calculations show that local cation intermixing confined to one interface can still sustain or enhance a 2DEG, whereas long-range "coherent" La/Sr intermixing across the superlattice largely removes the polar discontinuity and delocalizes the carriers, thereby suppressing the interfacial 2DEG.[17] Thus, cation substitution can help stabilize the interfacial electronic configuration but, depending on its spatial extent, can either assist or quench 2DEG formation.

D. Others

Beyond the electrostatic polar-catastrophe and growth-induced V_O-mediated doping, other class of mechanisms for oxide 2DEG formation and modulation relies on externally driven electrochemical rearrangements at or near the interface—chiefly field-assisted migration/redistribution of ionic defects in the capping oxide and near-interface substrate. These routes do not require a polar overlayer nor deliberate incorporation of V_O during growth; instead, they write, erase, or densify interfacial 2DEG after heterostructure fabrication.

One prominent example is gate-stimuli electro-migrative control, in which applied electric fields drive the migration or redistribution of mobile ionic defects. In amorphous-oxide/STO stacks, sufficiently strong negative gate biases (i.e., higher field, longer stress time, or elevated temperature) can substantially reduce the interfacial 2DEG density in a largely irreversible manner for a given history, consistent with field-assisted V_O migration from the interface into the gate oxide. Direct evidence for such electro-migrative processes has been provided by scanning transmission electron microscopy (STEM) combined with electron energy loss spectroscopy (EELS), which reveals a recovery of crystal-field splitting at the interface after stress, anchoring the electro-migrative picture.[40] At the nanoscale, biased conducting-AFM (CAFM) tips have been used to locally toggle the buried interface between insulating and conducting states—writing nanowires and cutting them with opposite bias [Fig. 4(a)]. The prevalent view is that the tip's intense local field triggers surface redox at the LAO top surface (e.g., removal/adsorption of oxygen). These sketch-defined FETs can then be drawn on demand, showing logic-like transfer characteristics, with features stable over many cycles.[41,42]

Structural distortion of the lattice offers an additional, and often intertwined, pathway to interfacial charge transfer. STEM-EELS on optimally annealed LAO/STO shows that the conducting interfaces exhibit c-elongated unit cells and head-to-head ferroelectric-like polarizations in both LAO and STO, whereas the subcritical stack remains nearly centrosymmetric; the resulting depolarization fields drive electron transfer into STO, forming a 2DEG.[43] In oriented LAO/STO (001)/(111) heterostructures, combined DFT and STEM

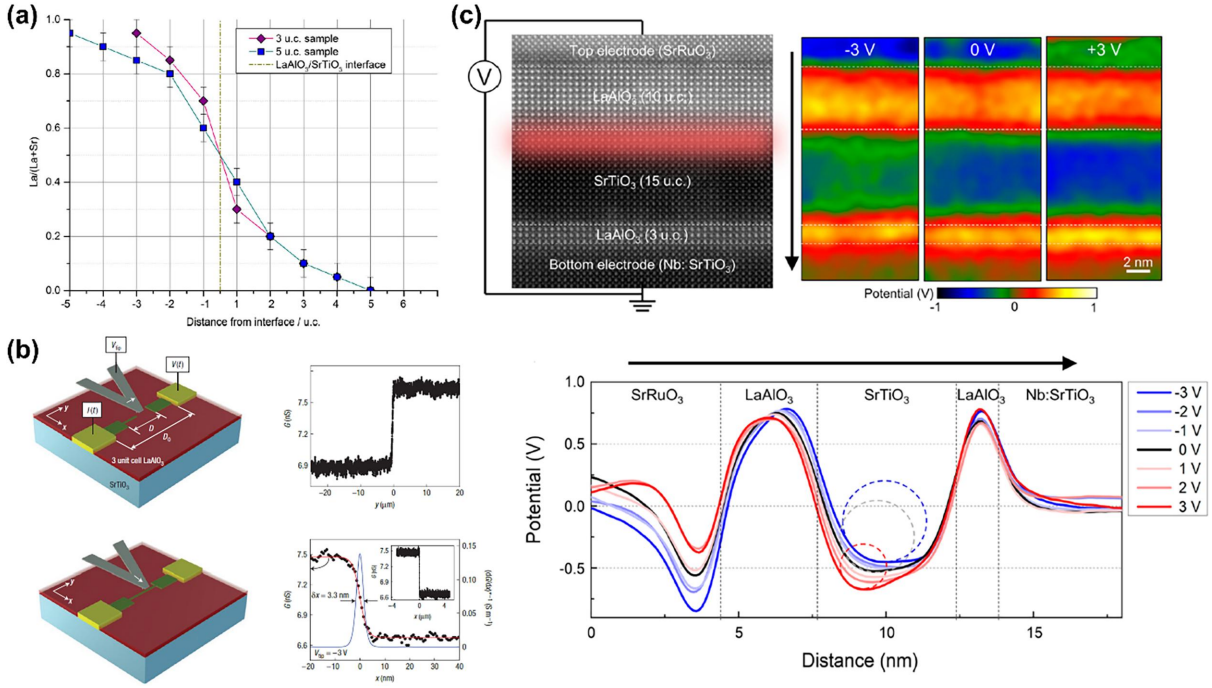

FIG. 4. Electric-field- and chemistry-assisted modulation of interfacial conduction in LAO/STO heterostructures. (a) MEIS measurements reveal finite La/Sr cation intermixing across the LAO/STO interface for ultrathin LAO films, indicating that localized chemical reconstruction can partially compensate polar discontinuity and modify the interfacial electronic landscape. Adapted with permission from H. Zaid *et al.*, Sci. Rep. **6**, 28118 (2016). Copyright 2016 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (b) A voltage-biased AFM enables reversible nanoscale writing and erasing of conducting channels at the buried LAO/STO interface, demonstrating highly localized, field-driven control of interfacial carrier density with nanometer-scale lateral confinement. Adapted with permission from C. Cen *et al.*, Nat. Mater. **7**, 298–302 (2008). Copyright 2008 Nature Publishing Group. (c) Inline electron holography under applied bias visualizes non-uniform redistribution of electrostatic potential across a gated LAO/STO device, with the strongest modulation localized on the STO side near the interface, consistent with electric-field-induced accumulation and depletion of the 2DEG. Adapted with permission from J. Seo *et al.*, Nat. Commun. **15**, 5268 (2024). Copyright 2024 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

work further reveals that FE distortions and nonpolar antiferrodistortive octahedral rotations are strongly coupled to the internal polar field and surface V_O.[44] More recently, *in situ* biasing experiments visualize that the electric field induces polar distortion in the LAO overlayer, modulating 2DEG [Fig. 4(c)].[45]

III. GENERATION OF OXYGEN VACANCIES AT INTERFACES

While polar discontinuity provides an idealized electrostatic framework for 2DEG formation, extensive experimental evidence has established V_O as a dominant and, importantly, engineerable source of interfacial carriers in oxide heterostructures. Unlike intrinsic electrostatic reconstruction, V_O-mediated charge donation is strongly influenced by growth conditions, processing environments, and external stimuli, rendering it highly amenable to deliberate control. As a result, the generation and manipulation of V_O have become central strategies for realizing oxide 2DEGs under scalable, CMOS-compatible conditions in both crystalline and amorphous systems.

In this section, we focus on the physical and chemical routes, by which V_O is introduced at oxide interfaces, emphasizing approaches that enable controlled, reproducible, and spatially localized V_O generation. These methods span direct physical processes, such as energetic particle bombardment, as well as chemically driven reduction or reactions during thin-film deposition and post-growth treatments. Together, they form the foundation for translating V_O-mediated 2DEG from incidental growth artifacts into intentionally engineered functional elements.

A. Ionic bombardment

Ionic bombardment processes, including energetic plasma exposure, ion milling, and Ar^+ irradiation, provide one of the most direct and controllable routes for generating V_O near oxide surfaces, thereby inducing a confined 2DEG. In this scenario, energetic ions preferentially sputter oxygen from the surface region of STO or related oxides, leaving behind a thin, oxygen-deficient layer that acts as an electron donor.

A prototypical demonstration of this mechanism showed that low-energy ion-beam preferential etching (IBPE) of STO(001) generates highly conductive 2DEG without a capping film [Fig. 5(a)].[46] The Ar^+ beam transforms the top few nanometers of insulating STO into a transparent conductor, whose resistivity at low T even drops below that of room-temperature copper, indicating a highly ordered, metallic conduction channel.

Subsequent *in situ* studies showed that Ar^+-bombarded STO surfaces made the evolution of this metallic surface more explicit.[47] Low-energy Ar^+ irradiation with *in situ* conductance measurement, irradiation developed steady-state oxygen deficient zone by the bombardment of argon ions. Under cryogenic conditions, the conductance saturates at specific value, while at high temperature, the conductance kept increasing, due to spontaneous thermal diffusion of V_O to the bulk region.

The microscopic evolution of this process has been elucidated through complementary local and spectroscopic probes. In Nb-doped STO, Ar^+ bombardment derives a transition from semiconducting state to a metallic state,[48] accompanied by the formation of conducting islands that eventually percolate into a continuous metallic layer once a critical fluence is reached, as visualized by local conductive AFM (LCAFM) [Fig. 5(b)]. XPS further reveals a progressive reduction of Ti from Ti^{4+} toward Ti^{3+} state with increasing fluence, directly linking metallic conduction to V_O-induced reduction.

Similar ionic bombardment strategies have been applied to other oxide substrates, deliberately engineering 2DEGs with controllable

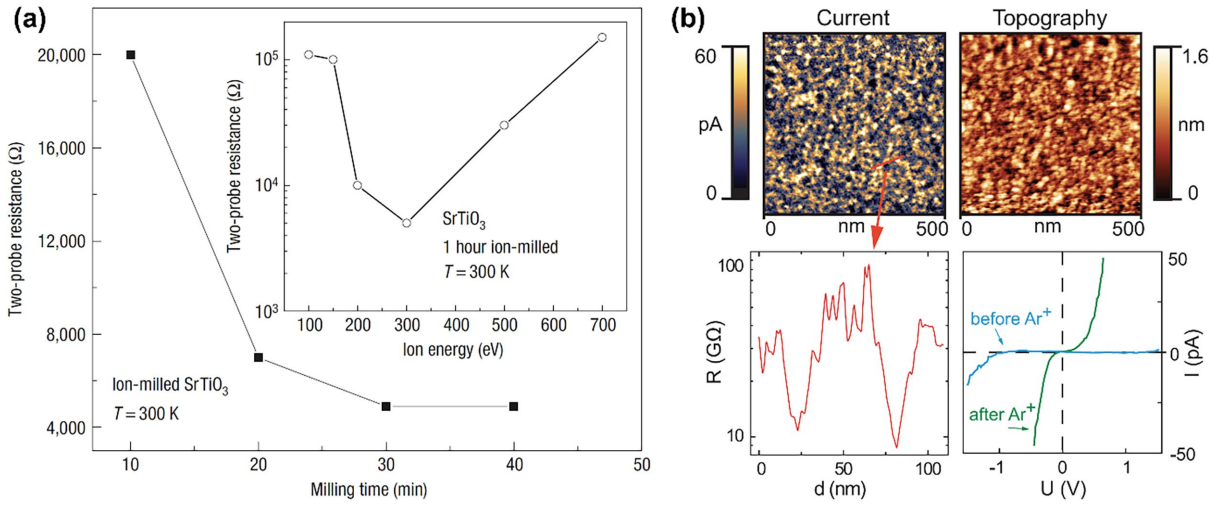

FIG. 5. V_O-mediated surface conduction in STO induced by ionic bombardment. (a) Two-probe resistance of STO decreases rapidly with increasing ion-beam exposure time and eventually saturates, indicating the formation of a stable, highly conductive near-surface layer created by preferential oxygen removal. The ion-energy dependence reveals an optimal low-energy window for efficient V_O generation without excessive lattice damage. Adapted with permission from D. W. Reagor and V. Y. Butko, Nat. Mater. **4**, 593–596 (2005). Copyright 2005 Nature Publishing Group. (b) Local-conductivity AFM measurements after Ar^+ bombardment show nanoscale electronic inhomogeneity with spatially distributed conducting regions. Line profiles and current–voltage characteristics confirm order-of-magnitude enhancement of local conductance, consistent with a V_O-induced insulator-to-metal transition confined to the surface region. Adapted from C. Rodenbücher *et al.*, Appl. Phys. Lett. **102**, 101603 (2013) with the permission of AIP Publishing.

depth and density. For example, anatase-TO grown on LAO substrate generates 2DEG layer with 4 nm-thickness by low-energy Ar^+ irradiation, demonstrating that ion-beam-induced V_O generation can be used to provide conducting interface across a range of oxide hosts.[49]

These controlled ion-irradiation experiments on nominally "bare" oxide crystals also provide important context for the long-standing debate over carrier origin in LAO/STO heterostructures. Based on transport, photoemission, and post-annealing studies, Siemons *et al.* explicitly argued that the large sheet carrier densities observed in many PLD-grown LAO/STO samples are predominantly due to extrinsic V_O-introduced by the pulsed-laser plume.[28] In their picture, the highly energetic ions and neutrals in the PLD plume play a role very similar to deliberate Ar^+ bombardment, knocking out oxygen from the STO surface during growth at low oxygen pressure. Thus, ionic bombardment-induced V_O provides a natural extrinsic explanation for many early LAO/STO samples with carrier densities far above 0.5 e/u.c. expected from ideal polar discontinuity.

B. Metal-induced redox reaction

Metal-induced redox reactions represent one of the most widely generalizable and experimentally robust mechanisms for generating 2DEG at oxide interfaces. This approach relies on the chemical reduction of bottom oxide substrates by reactive metal overlayers or redox-active oxide capping layers, which extract lattice oxygen and create V_O. These vacancies subsequently donate electrons that accumulate in a quantum-confined region at the interface, forming a 2DEG. The strength of this redox interaction is largely determined by the metal's enthalpy of oxide formation, deposition conditions, and overlayer stability.[50]

The redox process typically begins with the deposition of a highly reactive metal, such as Al, Fe, Eu, and Y, onto an oxide substrate. Owing to their strong oxygen affinities and relatively low work functions, these metals readily scavenge oxygen atoms directly from the substrate surface. Systematic studies have demonstrated that metals such as Al, Ta, and Y deposited on STO chemically reduce the substrate, forming corresponding metal oxides while inducing Ti^{3+} states. The extent of interfacial reduction correlates with the metal's oxidation enthalpy, following the trend $Y > Al > Ta$ in redox strength.[50]

Building upon this redox pathway, metal-induced reactions can also enable control over the type of interfacial carriers. At Fe/STO interface, the oxidation state of Fe plays a pivotal role: deposition of metallic Fe induces strong V_O creation in STO leads to a conventional n-type 2DEG, whereas deposition of oxidized Fe_3O_4 results in a p-type interface [Fig. 6(a)].[51,52] This redox-dependent switching between electron and hole gases highlights the sensitivity of interfacial reaction to chemical boundary conditions.

Among rare-earth metals, Eu exhibits one of the highest oxide formation enthalpies. Deposition of Eu metal on STO, which spontaneously forms EuO while simultaneously inducing V_O in the substrate, resulting in a spin-polarized 2DEG due to the proximity effect from the ferromagnetic EuO layer.[53,54]

Redox-mediated interfacial control is not limited to elemental metals but extends naturally to complex oxides. An amorphous $Sr_3Al_2O_6$ (*a*-SAO) was introduced as an overlayer on STO, where the Al component acts as the reducing species.[55] The V_O created beneath the *a*-SAO layer leads to a 2DEG, which can be completely erased by dissolving the SAO in water, thereby reoxidizing the substrate.

A simplified design rule for choosing redox-active metals is provided by the enthalpy-work function map.[56] Metals fall into distinct regions depending on how strongly they bind oxygen and whether their work functions lie below the electron affinity of STO. Metals with low work function and high formation enthalpy of oxide (e.g., Al, Ti, Hf, and Eu) readily scavenge oxygen from STO and are therefore ideal for inducing interfacial 2DEG. In contrast, high work function noble metals (e.g., Pt and Au) do not reduce STO and thus cannot generate redox-driven 2DEG [Fig. 6(b)].

Beyond STO-based heterostructures, redox reactions have also led to creation of 2DEG across a broader class of transition-metal oxides. Sputtering a thin Al film on to a (111)-oriented $KTaO_3$ produces a 2DEG via reduction of Ta^{5+} into Ta^{4+}/Ta^{2+}.[57] Likewise, replacing STO with anatase or rutile TO in amorphous-LAO heterostructures yields redox-driven 2DEG, while differences in 2DEG density and transport originate from changes in V_O diffusion activation energy at the substrate surface [Fig. 6(c)].[58] These results further establish metal-induced redox reactions as a broadly applicable and materials-agnostic strategy for engineering oxide 2DEGs.

Despite their versatility, metal-induced redox approaches also present several limitations. Compared to more controlled techniques such as ALD, the reaction-driven nature makes precise and reproducible control of carrier density challenging. In addition, the V_O-based origin can lead to stability and variability issues. These limitations motivate the need for more controllable approaches, as will be discussed in the following section.

C. Surface chemical reaction

Beyond the classical metal-induced reduction route to 2DEG formation, recent studies have revealed a variety of surface chemical reaction pathways. These processes include ALD-precursor-induced V_O formation, photon-stimulated defect chemistry, and interface-mediated oxygen exchange. Unlike energetic ion bombardment or direct metal deposition, such processes operate through localized chemical interactions at the growth interface, offering fine control over V_O generation under low-temperature and process-compatible conditions.

A seminal example of this approach was demonstrated by Lee *et al.* (2012), who demonstrated that ALD of certain oxides on STO can create a 2DEG at the interface via a ligand-driven chemical reduction mechanism.[34] In that study, amorphous LAO films grown by ALD at ~300 °C on TO-terminated STO were found to induce interfacial conduction (~10^{13} cm^{-2} carriers with mobility ~4–5 cm^2 V^{-1} s^{-1} at room temperature, increasing at low temperature). Notably, even non-polar, Al-containing oxides—amorphous AO and $YAlO_3$—produced a similar 2DEG on STO, whereas ALD of oxides lacking Al (e.g., Y_2O_3 and La_2O_3) under the same conditions did not yield conductivity. This pointed to the ALD precursor trimethylaluminum (TMA, $Al(CH_3)_3$) as the key agent: during the ALD half-cycles, the TMA's methyl ligands reduce the STO at the growth interface, abstracting oxygen and creating V_O that donate electrons into the STO conduction band [Fig. 7(a)].

Early *ex situ* studies suggested that a few ALD cycle with TMA and water vapor was required to form percolated conducting interface islands. Their study showed that the interface does not

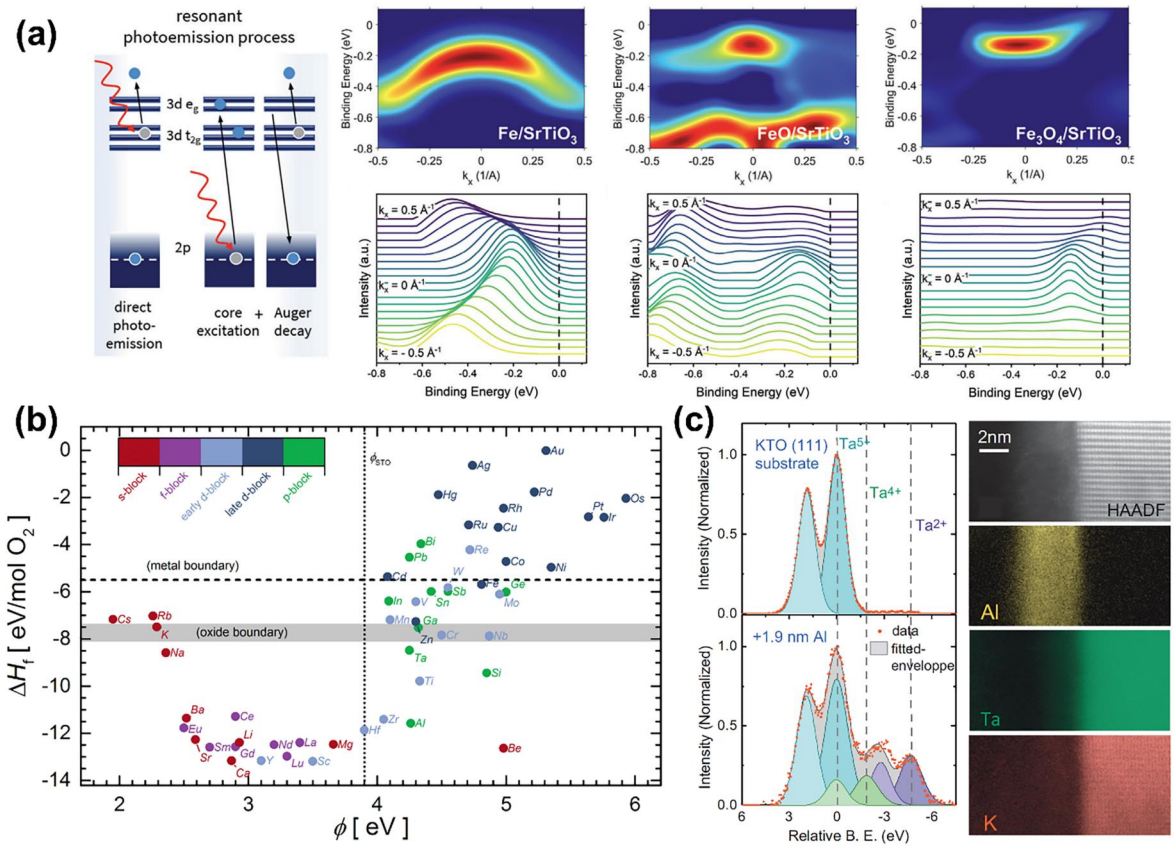

FIG. 6. Metal-induced interfacial redox reactions as a pathway to V_O-mediated 2DEG systems. (a) Resonant soft x-ray photoemission spectroscopy of Fe/STO interfaces reveals interface-induced electronic states within the STO bandgap, whose polarity is governed by the oxidation state of the Fe overlayer: metallic Fe stabilizes electron-like (n-type) interfacial states, whereas oxidized Fe promotes hole-like (p-type) states, demonstrating chemically switchable carrier polarity driven by interfacial redox chemistry. Adapted with permission from P. M. Düring *et al.*, Adv. Mater. **36**, 2309217 (2024). Copyright 2024 Wiley-VCH GmbH. (b) A materials-selection diagram correlating oxide formation enthalpy (ΔH_f) and metal work function (ϕ) classifies metallic overlayers on STO according to their propensity to induce interfacial redox reactions and V_O formation, identifying a regime favorable for confined 2DEG formation. Adapted from A. B. Posadas *et al.*, J. Appl. Phys. **121**, 105302 (2017) with the permission of AIP Publishing. (c) XPS and cross-sectional HAADF-STEM/EELS analysis of $AlO_x/KTaO_3$ interfaces directly visualize interfacial redox reactions, revealing reduced Ta valence states and atomically confined oxygen transfer with minimal cation interdiffusion, resulting in an electron-doped interfacial region. Adapted with permission from S. Mallik *et al.*, Nat. Commun. **13**, 4625 (2022). Copyright 2022 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

become uniformly conductive at once; rather, isolated metallic islands emerge and eventually coalesce, driven by non-uniform reduction across the substrate surface. This mechanism underscores the spatial inhomogeneity of ligand-induced reactions and highlights the importance of ALD parameters in achieving percolative conduction.[59]

This apparent threshold for conduction was later clarified through *in situ* electrical measurements. While *ex situ* studies suggested that multiple ALD cycles were necessary due to surface reoxidation upon air exposure, real-time monitoring revealed that a single TMA pulse alone is sufficient to drastically reduce the interfacial resistance and trigger spontaneous 2DEG formation [Fig. 7(b)].[37] The observed conduction emerges immediately after the first ligand-surface interaction, indicating that oxygen abstraction by TMA from the oxide substrate proceeds rapidly and locally, even before a full ALD cycle is completed. XPS further confirmed that Ti^{3+} signals were confined to the immediate interfacial region, demonstrating that the reduction is a surface-mediated chemical reaction, not driven by bulk diffusion. Notably, the formation of conducting paths still follows a percolative pattern, but the onset can be initiated by minimal ligand exposure when protected from ambient reoxidation.

Extending this concept from STO substrates to other oxide systems, the generality of ligand-driven surface reduction extends beyond STO to other reducible oxide semiconductors. Both amorphous and crystalline TO have been shown to support ALD-induced interfacial conduction when capped with AO, with pronounced differences arising from substrate crystallinity.[36,37] Notably, the anatase TO facilitated much stronger reduction and deeper carrier confinement compared to the amorphous phase, which showed shallower donor levels and localized carriers. This distinction stems from the difference in oxygen bonding environments, where ordered lattices allow more efficient oxygen abstraction.

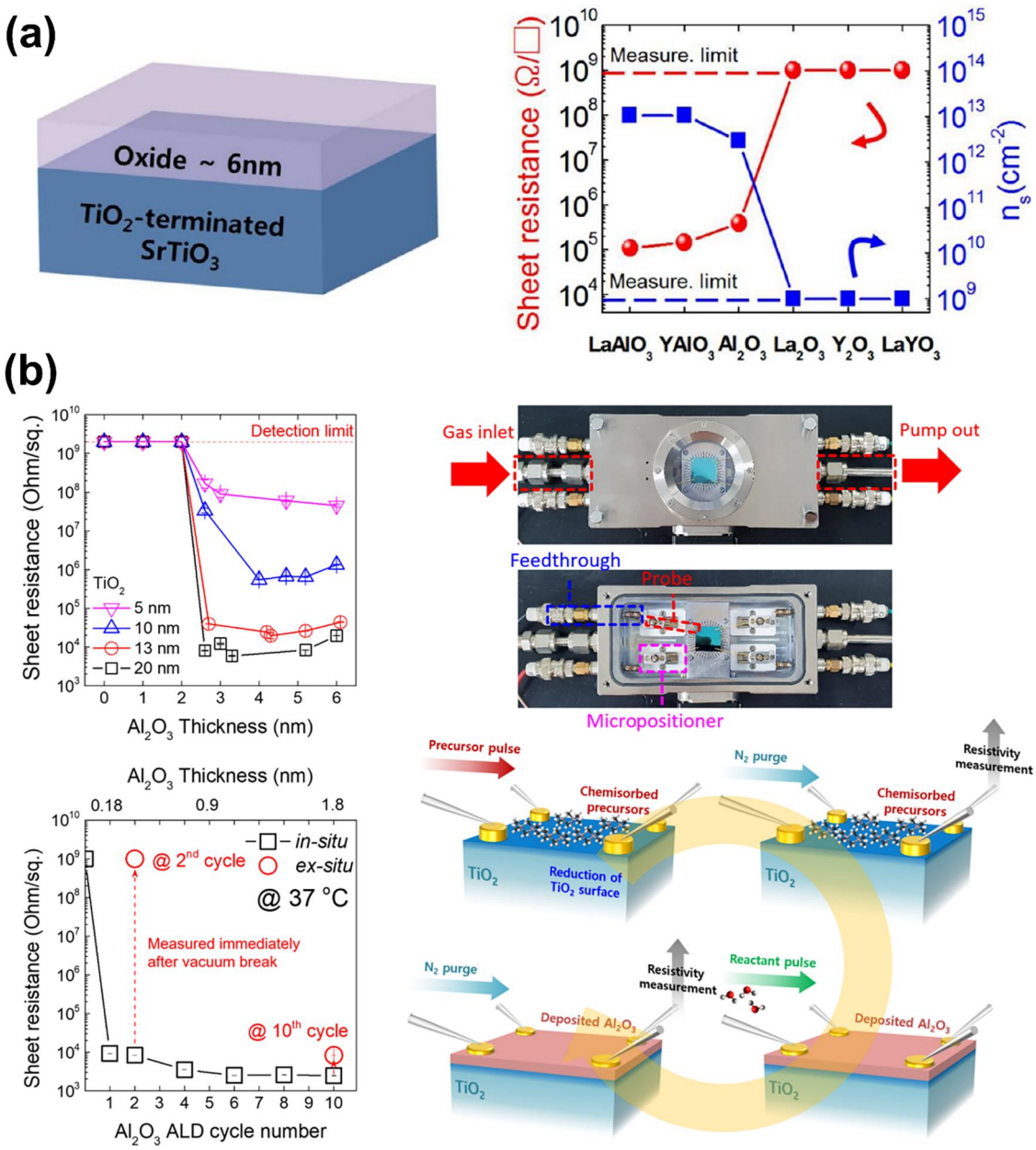

FIG. 7. Surface-chemistry-driven formation of 2DEG at amorphous oxide/STO interfaces. (a) Schematic and transport characteristics of amorphous oxide/TO-terminated STO heterostructures show that an ultrathin amorphous overlayer can induce interfacial conduction depending strongly on oxide chemistry: Al-containing amorphous oxides yield high-density conducting interfaces, whereas non-Al-based oxides remain insulating, underscoring the central role of interfacial redox reactions and V_O generation. Adapted with permission from S. W. Lee *et al.*, Nano Lett. **12**, 4775–4783 (2012). Copyright 2012 American Chemical Society. (b) *In situ* resistance measurements during ALD of AO on TO directly capture the creation of a 2DEG, revealing an abrupt insulator-to-metal transition beyond a critical overlayer thickness and demonstrating that the interfacial conduction is generated primarily during the initial TMA pulse via V_O formation. Reproduced with permission from T. J. Seok *et al.*, Chem. Mater. **32**, 7662–7669 (2020). Copyright 2020 American Chemical Society.

Similar ligand-induced interfacial 2DEG have been reported for IO[38] and ZnO,[60,61] materials widely used as amorphous or polycrystalline semiconductor channels. Upon deposition of AO, a significant increase in carrier density is observed, which is attributed to interfacial V_O formation triggered by chemical reduction. XPS analysis confirms the emergence of reduced cation states (e.g., In^{+}/In^{2+} and Zn^{+}), indicating that ligand-induced surface reactions effectively modulate the electronic structure of these wide-bandgap hosts.

In ZnO-based systems, the interplay between surface chemistry and microstructure becomes particularly evident. When ALD-AO was deposited on ZnO with a columnar grain morphology, the resulting 2DEG conduction was strongly modulated by the underlying grain structure.[61] Electron accumulation preferentially occurred in small lateral grain size, while grain boundaries acted as recombination centers, inducing lateral carrier localization. Furthermore, reducing the lateral grain size in vertically oriented ZnO films led to a measurable decline in carrier density, revealing that microstructural confinement imposes significant limits on V_O-mediated conduction pathways—even when interfacial chemistry is favorable.

Surface chemical redox reactions are not limited to ligand-driven processes and can also proceed through purely thermodynamic oxygen exchange between adjacent oxides. For example, deposition of IO onto AO has been shown to induce interfacial reduction, evidenced by depth-localized In^{1+}/In^{2+} states and Hall mobilities exceeding those of bulk IO.[62] In this case, the driving force was identified as a thermodynamic oxygen exchange from IO to AO, resulting in interfacial V_O accumulation without external reducing conditions. Furthermore, stacking multiple bilayers yielded additive enhancement in conductivity, underscoring the modularity of this interfacial reaction. These results indicate that 2DEG formation is fundamentally governed by interfacial thermodynamics rather than a specific process sequence, thereby enabling greater flexibility in device integration. In particular, such thermodynamically driven mechanisms open up broader opportunities for gate-first processing and Back-end-of-line (BEOL)-compatible 3D memory architectures.

Importantly, a key advantage of ALD-driven surface chemical reactions is their inherent tunability. By controlling precursor chemistry and process parameters, such as exposure sequence and treatment conditions, the interfacial carrier density can be modulated over several orders of magnitude, enabling deterministic control of electrical properties. This tunability has been leveraged in device demonstrations to realize distinct operation regimes within the same material platform,[35] and has also been demonstrated in scalable ALD-based systems through process-controlled modulation of interface conductivity.[63] Together, these examples indicate that while ALD ligand chemistry governs the redox initiation at the oxide interface, the substrate structure, including crystallinity, grain orientation, and even stacking direction, plays a decisive role in modulating the dimensionality and connectivity of the resulting 2DEG channel. This combination of chemical selectivity and structural tunability positions ALD-based surface redox as a key enabling strategy for scalable, low-temperature, and application-ready oxide 2DEG platforms beyond traditional perovskite systems.

IV. DEVICE APPLICATION

Chemically induced conductive oxide interfaces, particularly oxide 2DEGs, provide a distinctive materials platform for electronic devices. Unlike in conventionally doped semiconductors, the transport parameters of these interfaces, including carrier density and mobility, are defined within ultrathin CMOS compatible oxide stacks. Crucially, these metrics should not be treated as immutable material constants. Instead, they are state variables set by the interfacial defect configuration established during processing and maintained or modified during subsequent stabilization.

This perspective unifies a broad class of oxide 2DEG systems spanning epitaxial, polycrystalline, and amorphous heterostructures. Conductive channels can be realized not only in epitaxial LAO/STO but also in amorphous LAO/STO formed by PLD at room temperature, where electron densities up to $\sim 10^{14}\,cm^{-2}$ have been reported, and V_O is explicitly implicated as a dominant carrier source. In parallel, ALD-grown amorphous overlayers on STO offer a process-compatible route in which the 2DEG is commonly attributed to V_O created in STO during growth; for example, amorphous LAO grown by ALD produced $n_s \sim 10^{13}\,cm^{-2}$ with $\mu_{Hall} \sim$ a few $cm^2\ V^{-1}\ s^{-1}$, with electrons localized near the STO surface and the carrier source attributed to V_O. Consistent with this view, STO-based 2DEGs created by ALD span $n_s \sim 10^{13} - 10^{14}\,cm^{-2}$ with mobilities on the order of a few $cm^2\ V^{-1}\ s^{-1}$, overlapping with ranges reported for PLD/MBE-grown interfaces, reinforcing that the reported "numbers" are outcomes of an interfacial state rather than fixed constants.

Accordingly, Table I should be read as a state-space summary of chemically accessible interfacial conduction, not interpreted as a performance ranking: its values represent a range produced by the coupled action of (i) the defect-creation pathway (redox/vacancy generation set by the growth environment, notably thermal budget and oxygen chemical potential), (ii) the host oxide's intrinsic transport landscape (band structure/effective mass, crystallinity, trap spectrum and scattering), and (iii) interface stabilization/passivation that governs drift under air exposure, time, and temperature. A concrete illustration of the electrode-like limit in this state space is the *a*-AO/IO interface. In this system, ALD AO deposited on nanocrystalline IO forms a sub-3-nm metallic two-dimensional channel with relatively low R_{sh} and high ns, enabled by V_O confined near the interface and by an oxygen-extraction-induced semi-metallic InO_x phase. The channel remains air-stable for about one year because the AO overlayer provides effective passivation.

Beyond providing a conductive path, interfacial 2DEGs can be strongly coupled to adjacent oxides, which allows the same interface to serve different device functions depending on the selected interfacial state. For example, the 2DEG can operate as an electrostatically addressable channel, a localized defect or ion reservoir for switching, or an internal current limiting element. With this framing, we summarize how chemically formed oxide 2DEGs have been exploited in device applications. We begin with selector diodes and 2DEG-channel FETs, and then review memory implementations including 2DEG-enabled RRAM (CBRAM and VCM-type OxRAM, including mode-engineered variants), ALD-compatible capacitor-less 2T0C DRAM, and ferroelectric memories where the 2DEG serves either as an ultrathin channel under a ferroelectric gate (FeFETs) or as an oxide-compatible bottom electrode integrated at a ferroelectric/oxide interface (FRAM). Finally, we discuss neuromorphic-oriented examples, including neuransistors and ultrathin H_2 sensors as candidate sensory transducers for artificial olfactory neurons.

A. Selector

Crossbar-array (CBA) ReRAM offers a minimum cell footprint of $4F^2$, but in passive architecture it inherently suffers from sneak currents through unselected/half-selected cells, which degrades read margin and limits array scalability.[68] To mitigate this issue, a one-selector–one-resistor (1S1R) scheme integrates a selector in series with each memory element so that current is strongly allowed only in the selected state while being suppressed in half-selected states; more broadly, selector devices are introduced in crossbar arrays to suppress

TABLE I. Representative transport metrics of oxide-interface 2DEG systems. This table summarizes representative values of sheet carrier density (n_s), Hall mobility (μ_{Hall}), and sheet resistance (R_{sh}) reported for selected oxide-interface 2DEG systems across different material combinations and growth routes. The listed values are intended to provide a comparative overview of accessible transport regimes rather than a direct performance ranking. For entries marked as EDL-gated, the listed transport values were obtained under electric-double-layer gating rather than in the as-grown state.

Material	n_s ($\times 10^{13}$ cm^{-2})	μ_{Hall} (cm^2/V·s)	R_{sh} (Ω/sq.)	Condition
c-LAO/STO[14]	∼16	∼8.12	∼4.79×10^3	300 K
a-LAO/STO[34]	∼1	∼4–5	∼10^5	300 K
a-LAO/STO (PLD)[64]	∼12	∼9	∼6×10^3	300 K
Al/$KTaO_3$[57]	∼1		∼1.5 × 10^3	300 K
$GdTiO_3$/STO[65]	∼35	∼6.5	∼2.75 × 10^3	300 K
$NdTiO_3$/STO[66]	∼34			300 K
$LaInO_3$/$BaSnO_3$[67]	∼10	∼2100		Electric Double Layer(EDL)-gated, 10 K
a-AO/STO[34]	∼0.4	∼5	∼4×10^5	300 K
r-AO/STO[16]	∼2.3	∼27	∼10^4	300 K
a-AO/TiO_2[35]	∼10	∼2–5	∼10^4	300 K
a-AO/ZnO[60]	∼3	∼8.4	∼2.7×10^4	300 K
a-AO/In_2O_3[38]	∼50	∼20.5	∼850	300 K

sneak-path leakage while preserving sufficient current delivery to the selected cell.[69] In this context, three figures of merit are most commonly emphasized for selector assessment: (i) forward/reverse current ratio (F/R ratio), (ii) forward current density, and (iii) forward-bias nonlinearity, where nonlinearity is often quantified as $I(V_{read})/I(V_{read}/2)$.[70] As representative targets frequently cited for high-density CBA ReRAM, the selector should achieve F/R ratio, forward current density, and forward-bias nonlinearity.

1. Two-terminal (diode-type) selectors

a. Pt/a-AO/STO selector. Moon *et al.* demonstrated a diode-type selector in Pt/*a*-AO/(2DEG)/$SrTiO_3$ stacks by exploiting intrinsically asymmetric band alignment: a high Schottky barrier at the Pt/*a*-AO interface serves as the blocking contact, whereas the *a*-AO/2DEG junction behaves as a quasi-Ohmic contact. The resulting device exhibits rectification with an abrupt forward turn-on at ∼0.5 V (Pt positive), achieving a maximum forward/reverse current ratio (F/R ratio) of ∼10^4 [Fig. 8(a)]. The forward-bias nonlinearity reaches ∼10^3 at $|V| = 1.5$ V, and these rectifying characteristics remain stable under repeated bipolar pulsing (± 1.5 V, 20 ms) up to 10^3 cycles, indicating robust endurance of the MIM-type selector stack. Beyond the static I–V nonlinearity, time-dependent resistance evolution was attributed to field-driven V_O redistribution near the *a*-AO/2DEG interface, which modulates the effective barrier and leakage under bias stress. It is also noteworthy that the measured forward conduction is accompanied by a relatively large series resistance of ∼850 KΩ, extracted from the high-positive-bias region, reflecting the limited conductivity of the 2DEG current path rather than an intrinsically low-resistance selector state. Accordingly, while the device clearly demonstrates selector functionality, its on-state resistance remains too high for direct consideration as a high current selector in dense crossbar arrays, where large forward current density is a key requirement. Therefore, the significance of this work lies primarily in establishing chemically induced oxide 2DEGs as conductive, interface-engineerable bottom electrodes whose band alignment can be exploited to realize diode-type selector behavior, while also revealing that reduction of parasitic series resistance is essential for practical implementation.[71]

b. Pt/a-AO/Nb:STO selector. Building on the Pt/*a*-AO/STO diode, Moon *et al.* replaced the interfacial 2DEG with a degenerate Nb:STO bottom electrode while keeping the ultrathin ALD *a*-AO layer (4 nm). Removing the 2DEG-related series resistance enabled substantially larger forward current (approaching the measurement limit) and markedly improved key selector metrics: both the F/R ratio and forward-bias nonlinearity reached the order of 10^6 at ∼1.2 V. In addition, a reverse-bias positive temperature coefficient of resistance (PTCR) behavior further suppressed leakage at elevated temperature, pushing the F/R ratio toward ∼10^7 at 70 °C. Mechanistically, the forward branch was interpreted as being consistent with trap-assisted tunneling through the *a*-AO barrier.[70] Importantly, the reverse-leakage physics in Pt/*a*-AO/(Nb:)$SrTiO_3$ stacks appears to be governed strongly by oxide defects rather than solely by the perovskite electrode: Kornblum *et al.* reported that leakage in Pt/*a*-AO/(Nb:)$SrTiO_3$ is dominated by defect-mediated transport in the as-deposited state (trap-related conduction such as Poole–Frenkel and/or trap-assisted processes), whereas post-deposition annealing reduces the defect contribution and drives the transport toward Fowler–Nordheim tunneling. They further noted that the interfacial electronic structure did not necessarily indicate V_O-dominated interfacial states (e.g., lack of Ti^{3+} signatures), reinforcing that the dominant leakage channel is frequently set by the *a*-AO defect landscape and processing conditions. Taken together, these studies show that reverse leakage in ultrathin ALD AO diodes is primarily governed by trap states in the AO layer and can be tuned by deposition conditions and post-deposition annealing, thereby determining selector performance. In the CBA context, these results indicate that improving bottom-electrode conductivity is not merely beneficial for increasing

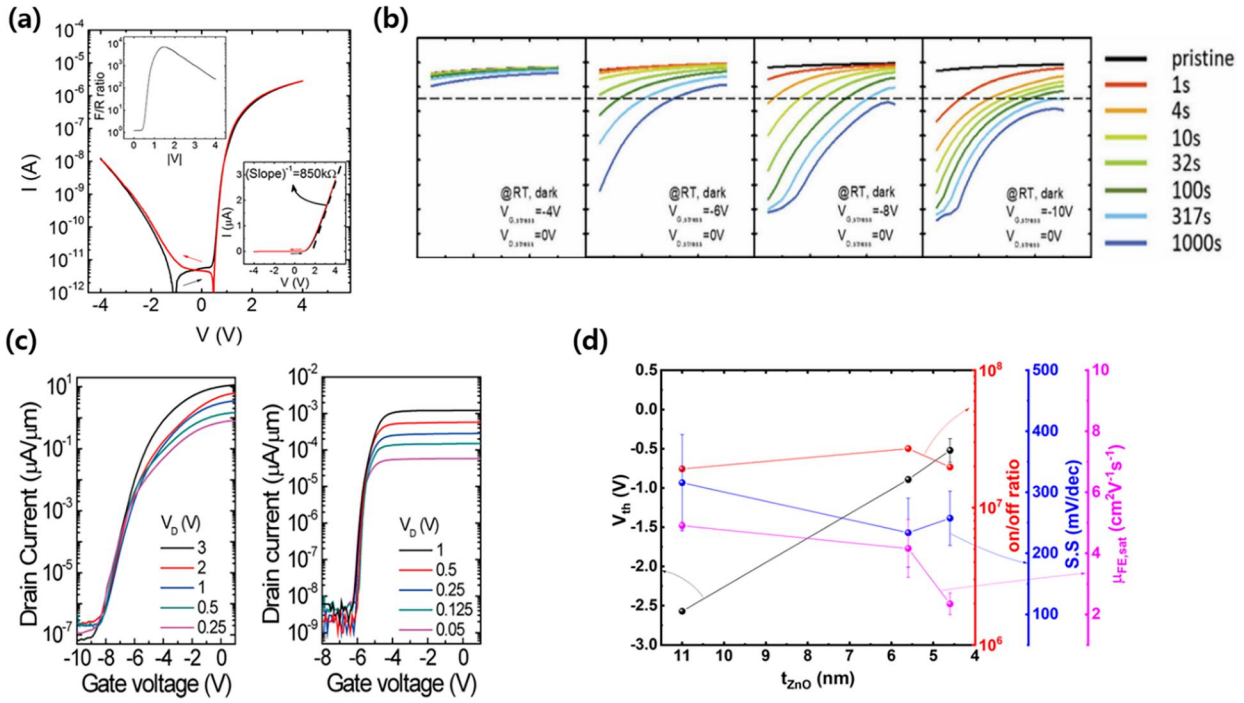

FIG. 8. Representative electrical characteristics of oxide 2DEG–based selectors (two-terminal diodes and three-terminal FET-type devices). (a) Pt/a-AO/2DEG/STO diode selector I–V curves measured as-fabricated and after electrical stress; inset shows the forward/reverse (F/R) ratio vs |V|. Adapted from T. Moon *et al.*, APL Mater. **5**, 042301 (2017). Copyright 2017 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (b) Transfer curves of a Pt/a-AO/2DEG/STO FET under negative gate-bias stress ($V_d = 0$), showing progressive current suppression and Vth shift with increasing stress duration and magnitude. Adapted with permission from T. Moon *et al.*, Adv. Electron. Mater. **6**, 1901286 (2020). Copyright 2020 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (c) Transfer characteristics of ALD-grown a-AO/TO quasi-2DEG FETs measured under different drain biases, comparing higher-density and lower-density devices. Adapted with permission from T. J. Seok *et al.*, ACS Nano **12**, 10403–10409 (2018). Copyright 2018 American Chemical Society. (d) a-AO/ZnO 2DEG FET thickness dependence, showing extracted trends of V_{th}, on/off ratio, SS, and $\mu_{FE,sat}$ vs t_{ZnO}. Adapted with permission from H. J. Lee *et al.*, ACS Appl. Electron. Mater. **3**, 3247–3255 (2021). Copyright 2021 American Chemical Society.

the absolute forward current but is also important for making ultra-thin ALD-oxide selectors more relevant to 1S1R operation, where sufficient current delivery and suppressed half-select leakage must be achieved simultaneously. At the same time, the strong dependence of reverse leakage on defect-mediated transport highlights that selector optimization in such structures cannot rely on electrode design alone but also requires careful control of the AO defect landscape and post-deposition processing.[72]

2. Three-terminal (FET-type) selectors

Three-terminal (FET-type) selectors add an electrostatic control knob via the gate, enabling deliberate tuning of the OFF state while preserving usable ON current for array operation. In these devices, conductance is governed by electrostatic modulation of the 2DEG channel, whereas in two-terminal structures it is primarily dictated by field-driven transport across the oxide layer. At the same time, oxide 2DEG transistors should not be regarded as selector-only devices. Depending on the material platform and integration scheme, they are also relevant to broader thin-film transistor and oxide-electronics applications, including logic-oriented and integrated-device concepts. We specifically focus on threshold-voltage (V_{th}) control via carrier-density modulation in oxide 2DEG channels across different hetero-oxide platforms, because the dominant shared bottleneck across these devices is the strong depletion-mode tendency caused by the intrinsically high interfacial carrier density. This issue directly governs OFF-state controllability, standby-power penalty, and the practical usability of the channel. The representative device metrics are summarized in Table II.

a. a-AO/STO FET. In top-gated Pt/*a*-AO/STO transistors, the as-formed *a*-AO/STO interface can host a high-density 2DEG, making the channel difficult to deplete within a practical gate-bias range; Moon *et al.* therefore applied a strong negative gate-bias stress to reduce the effective carrier source and to shift the channel response from metallic-like weak modulation to semiconducting-like behavior, consistent with the sharp current drop near ∼−6 V and the emergence of a conventional semiconducting C–V response after stressing. Figure 8(b) shows how the transfer curve evolves under negative gate stress: at $V_{G,stress} = -4$ V, the curve changes little even with long stress time, while stronger stress (−6 to −10 V) and longer time (1–1000 s) progressively shift the transfer curves toward higher V_G, giving a clear positive V_{th} shift and a more defined subthreshold region; for example, using a constant-current definition, V_{th} after 100 s shifts from −2.81 V at (−6, 0) to −0.76 V at (−8, 0) V, and after sufficient stressing (e.g., −8 V, 1000 s) SS reaches 0.495 V/dec. These trends are

TABLE II. Key transistor metrics of oxide 2DEG FETs (three-terminal, FET-type selector devices). This table compiles representative threshold voltage (V_{th}), subthreshold swing (SS), on/off current ratio (I_{on}/I_{off}), and effective mobility (μ_{eff}) reported for oxide 2DEG transistors based on amorphous-AO. The values provide a concise comparison of gate controllability and switching performance across different channel stacks and process conditions (h-FET vs l-FET). All films, except for STO substrates requiring high-temperature treatment, were processed using low-temperature (<300 °C) ALD.

	V_{th} (V)	SS (mV/dec)	I_{on}/I_{off}	μ_{eff} ($cm^2/V{\cdot}s$)
a-AO/STO [40]	−1.31	495	1.6×10^5	
a-AO/c-TO (h-FET)[35]	−3.7	485	10^8	3.53
a-AO/c-TO (l-FET)[35]		<100	10^6	2.79
a-AO/c-ZnO[61]	−0.86	194	10^7	4.8

attributed to V_O being driven away from the interfacial region into the *a*-AO bulk, which lowers the 2DEG carrier density and makes depletion feasible. A small positive drain bias during stress can assist once the channel begins to deplete [e.g., (−6, 2) V gives $V_{th} = -1.39$ V], but a too-large drain bias tends to keep the channel conductive and screens the field, reducing the net conditioning and potentially worsening degradation. In summary, negative gate-bias stress provides a practical knob to tune the 2DEG carrier density and V_{th} via V_O motion, but the stress conditions should be chosen to gain V_{th}/SS improvement without excessive on-current loss and stability penalty.[40]

b. a-AO/TO FET. Unlike *a*-AO/STO, the *a*-AO/TO platform enables a quasi-2DEG channel in fully ALD-processed, ultrathin oxide stacks on SiO_2/Si without requiring a single-crystal channel, making it attractive for scalable thin-film 2DEG FETs.

Seok *et al.* exploited the thermally activated TMA-driven reduction (V_O generation) as a control knob by fabricating top-gated transistors with an ultrathin TO (∼7 nm)/AO (∼2.5 nm) channel stack and tuning the ALD AO deposition temperature (280 °C vs 230 °C). Because TMA acts as a strong reducing agent, chemical reduction during AO ALD generates interfacial V_O that donates electrons to the quasi-2DEG, providing a direct microscopic basis for the strong temperature dependence of carrier density. With higher AO process temperature, the transfer curve shows a much more conductive channel with weaker gate control, consistent with a deeper depletion-mode behavior: the device exhibits a negative V_{th} ($V_{th} \sim -3.7$ V) and a relatively large SS (∼485 mV/dec). In contrast, the low-density device (l-FET) shows near-full depletion of the ultrathin TO channel, with a clear turn-off and a much steeper subthreshold response (SS < ∼100 mV/dec) at the expense of reduced on-current [Fig. 8(c), left: h-FET; right: l-FET]. These results establish a clear tradeoff: stronger reduction increases electron density and conductance but shifts V_{th} more negative and makes full electrostatic turn-off harder unless the carrier density is deliberately limited.[35]

Beyond reduction strength, later mechanistic studies indicate that TO crystallinity (thickness and/or post-deposition annealing) provides a second lever by reshaping V_O-related donor energetics, which changes the mobile electron density and, consequently, the V_{th} tendency. Seok *et al.* reported that improving TO crystallinity (e.g., increasing thickness from 5 to 10/13 nm) lowers the donor activation energy from ∼189 to ∼27 meV/∼18 meV, while an annealed 5 nm TO also showed a reduced activation energy (∼99 meV).[37] A key point is that V_{th} follows the mobile-carrier density, not simply the total V_O density: even if the V_O concentration decreases with increasing crystallinity, shallower donors increase the fraction of thermally ionized electrons at room temperature, which can raise the mobile electron density and drive V_{th} more negative unless intentionally managed. Complementarily, Lee *et al.* showed that highly disordered (very thin) TO can generate many electrons that are captured by deep traps (large discrepancy between ARXPS-estimated and Hall-measured n_s), whereas improved crystallinity via PDA reduces this discrepancy, consistent with a reduced deep-trap density and a larger mobile-carrier fraction.[36] Taken together, *a*-AO/TO 2DEG FETs offer two coupled V_{th}-control axes: (i) reduction strength (process temperature) that sets the overall carrier density and depletion-mode tendency, and (ii) TO crystallinity that tunes donor shallowness/trapping, which can further increase mobile electron density and drive V_{th} more negative unless intentionally managed.

c. a-AO/ZnO FET. Among fully ALD-processed hetero-oxide 2DEG channels on SiO_2/Si, the *a*-AO/ZnO platform is particularly attractive because it can achieve higher Hall mobility than TO-based stacks, consistent with ZnO's smaller conduction-band electron effective mass (∼0.24 m_0) and the stronger effective-mass and polaron-related mobility limitations typically associated with TO.

Lee *et al.* intentionally grew ZnO under highly oxygen-rich ALD conditions (DEZ/O_3), rendering the bulk ZnO film highly insulating; accordingly, the measured conduction after *a*-AO capping was attributed to interfacial 2DEG formation rather than bulk ZnO leakage. ARXPS indicates that V_O-related reduced states are confined to approximately 0.62 nm into ZnO from the *a*-AO/ZnO interface. The authors attributed this sharp confinement, supported by ZnO crystallinity even on amorphous SiO_2, to a reduced tendency for V_{th} to shift excessively negative. A representative top-gated *a*-AO/ZnO 2DEG FET nevertheless still exhibited a negative threshold voltage (≈−2.4 V), motivating explicit V_{th} engineering.[60]

A practical and clearly demonstrated V_{th}-control lever is ZnO thickness (microstructure) scaling. In the sub-10-nm regime, decreasing t_{ZnO} (11 → 4.6 nm) reduced the lateral grain size and increased grain-boundary (GB) density, where GB-induced deep acceptor-like traps capture 2DEG electrons and thereby lower the effective sheet carrier density n_s, shifting V_{th} positively from −2.6 to −0.63 V [Fig. 8(d)]. Figure 8(d) also indicates that this ns reduction improves gate control: as t_{ZnO} is reduced from 11 nm toward ∼5–6 nm, SS decreases to the ∼200 mV/dec range, and the on/off ratio rises into the 10^7 regime, consistent with a suppressed I_{off} via more complete depletion. When t_{ZnO} is further reduced to 4.6 nm, V_{th} continues to shift positively, but $\mu_{FE,sat}$ drops markedly (to ∼2.5 $cm^2\ V^{-1}s^{-1}$) and SS slightly increases (226 mV/dec), consistent with abundant GBs adding carrier scattering/transport barriers that reduce I_{on} even though I_{off} remains very low. With an optimized $t_{ZnO} \approx 5.6$ nm, the device reached $V_{th} \approx -0.86$ V while maintaining high on/off (∼2.7 × 10^7) and SS (∼194 mV/dec). Importantly, this approach is not "preventing" GB traps; rather, it uses GB-mediated trapping as an electrostatic lever to reduce effective ns and relax depletion-mode

operation—at the cost that overly strong ns reduction can also degrade on-current, so the tradeoff must be tuned around the target V_{th} window.[61]

Across the various material systems discussed above, the V_{th} spans a wide range depending on the interfacial carrier density and defect chemistry. From a device perspective, however, a V_{th} close to 0 V is desirable for low standby power operation. In most oxide 2DEG transistors, V_{th} tends to be negative due to the high interfacial carrier density originating from V_O. Several strategies have been proposed to shift V_{th} toward positive values, including suppression of V_O formation through oxidizing growth or reducing the interfacial redox reaction (i.e., lower-temperature ALD), electrostatic control via ultrathin channel design enabling full depletion, and dipole engineering of the gate dielectric to modulate the band alignment and carrier density.[73] These approaches provide viable pathways toward enhancement-mode 2DEG devices.

B. Memory

1. Dynamic memory

Conventional 1T1C DRAM scaling is increasingly constrained by the footprint and leakage of the storage capacitor, pushing the capacitor toward extreme aspect ratios and tighter leakage/variability budgets as density increases.[74] These pressures have renewed interest in two related but distinct routes toward higher density: monolithic 3D (M3D) integration through vertical stacking, and capacitor-less gain-cell concepts such as 2T0C DRAM, which store data as charge on the read-transistor gate-oxide capacitance and remove the explicit capacitor from the cell layout.[75] Oxide-semiconductor channels, such as indium gallium zinc oxide (IGZO), are widely explored in this context because they can offer low off-state current and process/stacking flexibility, while ALD-based routes provide conformal and thickness-controlled films that are attractive for vertically integrated device architectures.[76] In aggressively scaled and monolithically stacked 2T0C arrays, however, retention is often limited not only by channel I_{off} but also by leakage through gate/dielectric stacks and other parasitic discharge paths. This shifts the practical question toward channel electrostatics, namely, which channel configuration can most robustly enforce a deeply depleted off state and suppress storage-node discharge under stacking-induced leakage.

To address this electrostatic bottleneck, an interface-confined 2DEG provides an ultrathin, 2D-like conduction channel that can be more effectively depleted by the gate, thereby suppressing storage-node discharge even when stacking introduces additional leakage paths. Figure 9(a) schematically illustrates the vertically stacked 2T0C architecture based on Al_2O_3/TiO_2 2DEG transistors; the 2DEG is the interfacial channel formed locally between source and drain in each transistor, while the global substrate back-gate bias used in the measurements is not explicitly drawn in the simplified schematic. In this platform, the active conducting region is confined to only a few nanometers from the interface, consistent with the strong interfacial confinement that distinguishes oxide 2DEG channels from more conventional oxide-semiconductor channels and underlies their electrostatic advantage. In practice, leveraging a strongly confined channel that can be fully depleted enables steep switching (SS $\approx$ 100 mV/dec) and an extremely low I_{off} ($< 2 \times 10^{-17}$ A/μm) at the transistor level; at the 2T0C cell level, making VBG more negative extends retention from $\sim$100 to $\sim$400 s while maintaining an ultra-low extracted leakage current ($\sim 2 \times 10^{-17}$ A/μm), consistent with biasing the write transistor deep into the off state so that carriers are depleted both at the interface and throughout the ultrathin TiO_2 film. The same results also define a practical bias window, because excessively negative VBG can increase gate leakage via electron drift toward the top-gate dielectric. Finally, leveraging ALD conformality and thickness control, they monolithically stacked two 2T0C layers; despite stacking-induced defects and leakage paths, the first and second layers still retained data for $\sim$30–40 and $\sim$4–5 s, respectively, indicating that oxide 2DEG channels are a promising material option for M3D capacitor-less DRAM, while further improvements in parasitic-leakage suppression, dielectric reliability, and lateral/interconnect scaling remain necessary for future development.[77]

2. Ferroelectric memory

a. FeFET. A ferroelectric field-effect transistor (FeFET) stores information as a threshold-voltage shift induced by the remanent polarization of a ferroelectric gate stack. This ultrathin and strongly confined channel becomes especially important in FeFETs because erase completeness and the memory window (MW) are ultimately limited by the voltage that drops across the ferroelectric during program and erase. In Si-based FeFETs, an unavoidable low-k interfacial SiO_x layer formed during ferroelectric processing can introduce charge trapping and consume part of the applied voltage, shrinking the effective field across the ferroelectric and reducing MW.[78] Even when oxide channels are adopted to avoid the Si interfacial-layer penalty, erase can remain weak because many oxide semiconductors are strongly n-type; the scarcity of hole minority carriers can leave the channel potential partially floating during erase, again reducing the voltage drop across the ferroelectric and collapsing MW.[79]

Seo *et al.* addressed this electrostatic bottleneck by adopting an ultrathin oxide 2DEG channel at the TiO_x/AlO_x interface, where the conducting sheet is tightly confined and can be readily depleted to avoid a floating-channel condition and enable complete erase [Fig. 9(b)]. The FeFET achieves an MW of $\sim$4.2 V, approaching the theoretical maximum, and preserves a similarly large MW even at a 1 μs pulse width. The MW changes by less than 3% after 10^9 program/erase cycles, and retention at 85 °C is $\sim 10^4$ s with 10-year retention extrapolated. These results indicate that an interface-confined 2DEG channel can restore efficient ferroelectric voltage coupling without compromising reliability.[80]

In this framing, DRAM and FeFET can be connected by one shared message: chemical-reduction-enabled oxide 2DEGs provide an interfacially confined, readily depletable channel that: (1) strengthens depletion to suppress retention-limiting leakage in stacked 2T0C storage under dual-gate control; and (2) prevents the "floating channel potential" bottleneck in n-type oxide FeFETs, restoring erase completeness and expanding MW toward the theoretical limit.

b. FRAM. A ferroelectric random-access memory (FRAM) stores information directly in the remanent polarization state of a ferroelectric capacitor, rather than in the threshold shift of a transistor channel. Whereas the FeFET above places a ferroelectric gate stack on top of a separately engineered conductive channel, the $Hf_{0.5}Zr_{0.5}O_2$ (HZO)/STO FRAM work demonstrates a more co-located strategy in

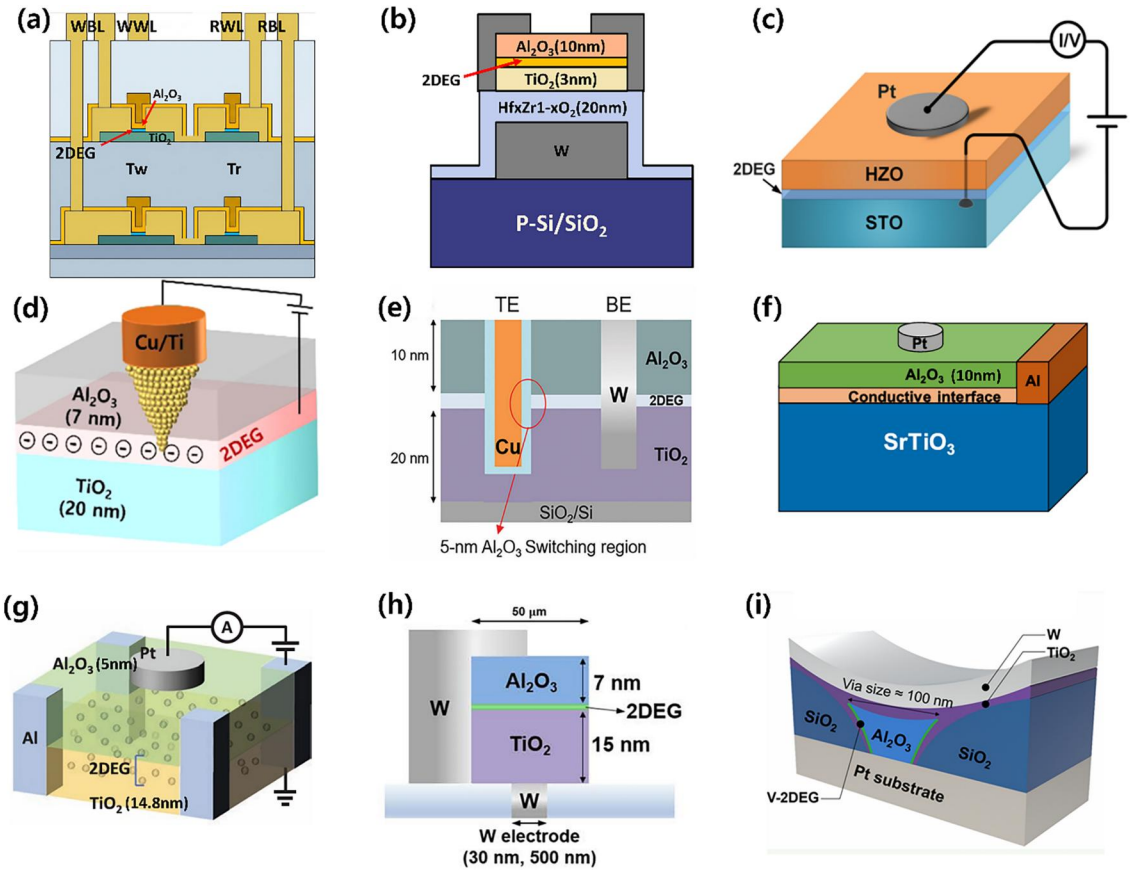

FIG. 9. 2DEG-enabled memory devices: DRAM, ferroelectric memory, and resistive memory(architectures and representative characteristics). (a) Schematic cross-sectional view of a vertically stacked 2T0C DRAM cell based on Al_2O_3/TiO_2 interface-channel FETs, where the 2DEG is locally formed in each transistor channel. (b) 2DEG FeFET gate stack (W/HZO/TOx/AOx with an interfacial 2DEG channel). (c) Pt/HZO/2DEG/STO capacitor-type FRAM structure using the interfacial 2DEG as the bottom electrode. Adapted from H. Yu *et al.*, Appl. Phys. Lett. **127**, 201601 (2025) with the permission of AIP Publishing. (d) Planar Cu-based CBRAM structure on an AO/TO stack integrating a 2DEG layer at the AO/TO interface. Adapted with permission from S. M. Kim *et al.*, ACS Appl. Mater. Interfaces **11**, 30028–30036 (2019). Copyright 2019 American Chemical Society. (e) Vertical CBRAM (V-CBRAM) structure combining a confined AO switching region with a lateral 2DEG layer in a compact vertical geometry. Adapted with permission from J. Kim *et al.*, Adv. Electron. Mater. **11**, 2400650 (2025). Copyright 2025 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (f) Pt/AO/STO structure incorporating a conductive interface at the AO/STO boundary. Adapted from D. Miron *et al.*, Appl. Phys. Lett. **116**, 223503 (2020) with the permission of AIP Publishing. (g) Planar Pt/AO/TO structure with a 2DEG layer at the AO/TO interface. Adapted with permission from Y. Li *et al.*, Adv. Electron. Mater. **9**, 2200800 (2023). Copyright 2023 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (h) Scaled W/AO/TO/W cell (representative nm-scale oxides) integrating the AO/TO interfacial conductor within the stack. Adapted with permission from J. Kim *et al.*, Nanotechnology **35**, 025205 (2024). Copyright 2024 IOP Publishing Ltd. (i) Via-defined vertical architecture integrating a nanoscale vertical 2DEG (V-2DEG) region within a compact 3D cell geometry. Adapted with permission from J. Kim *et al.*, ACS Appl. Electron. Mater. **5**, 6178–6188 (2023). Copyright 2023 American Chemical Society.

which ferroelectricity and interfacial conduction are engineered at the same oxide heterointerface. A metallic 2DEG formed at the HZO/STO boundary is directly employed as an inherent bottom electrode in a Pt/HZO/2DEG/STO capacitor [Fig. 9(c)], enabling an oxide-only ferroelectric memory stack without inserting an additional bottom metal at the functional interface. Importantly, the study maps a deposition-temperature/oxygen-pressure window that preserves both ferroelectric switching and metallic interfacial transport, indicating that the same interfacial defect chemistry that stabilizes the 2DEG can also be used to co-optimize leakage/transport and ferroelectric response. This makes the interface a tunable knob that simultaneously sets electrode quality (2DEG transport/leakage) and ferroelectric switching. In the optimized stack, clear polarization hysteresis is obtained with a maximum remanent polarization $P_r = 14.7\ \mu C\ cm^{-2}$ at a 5 V drive (1 kHz).[81] At the same time, the present study is primarily a proof-of-concept capacitor demonstration, and detailed endurance and retention benchmarks comparable to those reported for the FeFET have not yet been established.

Conceptually, this reframes chemically stabilized oxide 2DEGs not merely as transistor channels, but as intrinsic electrodes: an interface-defined conducting sheet that can simplify ferroelectric capacitor stacks without sacrificing electrostatic leverage. When integrated with ferroelectric HZO, the same oxide interface can be engineered so that 2DEG formation/depletion and polarization switching

are co-optimized, enabling a compact all-oxide stack that simultaneously offers a robust conductive pathway and nonvolatile ferroelectric memory functionality.

3. Resistive memory

Resistive random-access memory (RRAM) comprises two-terminal metal–insulator–metal (MIM) cells whose resistance is reversibly tuned by electrically driven ionic motion and redox reactions.[82] Canonical redox-based RRAM mechanisms include (i) electrochemical metallization (ECM/CBRAM), where Ag/Cu cations migrate and form/dissolve a metallic conductive bridge, (ii) valence-change memory (VCM), where oxygen-ion (equivalently V_O) redistribution locally reduces/oxidizes the oxide and modulates conductivity, and (iii) thermochemical (fuse/antifuse) switching, where Joule heating induces local chemical modification and often manifests as unipolar behavior.[83,84] In most oxide implementations, the ON state is dominated by a nanoscale, localized conductive filament rather than a homogeneous change, and the stochastic nature of filament nucleation/growth/rupture broadens forming/SET/RESET distributions and degrades cycle-to-cycle and cell-to-cell uniformity.[85,86]

2DEG-enabled RRAM leverages conductive oxide interfaces as electrodes and controllable defect/ion reservoirs, offering a materials-level route to alleviate the intrinsic variability of conventional filamentary memories.[87,88] In both ECM/CBRAM and VCM-type Oxide-based RRAM (OxRAM), the 2DEG concept provides a means to confine and regulate the active defect/ion population at the switching region, which can translate into more stable operating voltages and improved switching uniformity.[89,90] More recently, conductive oxide interfaces have also been explored as defect reservoirs to better control V_O concentration/distribution, motivating a shift toward more uniform trap-controlled operation such as space-charge-limited conduction (SCLC) switching in scaled cells.[91] Accordingly, this section first reviews representative 2DEG-assisted ECM/CBRAM and then discusses 2DEG-enabled VCM-type OxRAM (including non-filamentary variants), focusing on how the 2DEG-as-electrode/reservoir paradigm impacts switching uniformity and key operating metrics, which are summarized in Table III.

a. CBRAM. Conventional Cu-based CBRAM often suffers from uncontrolled filament thickening and current overshoot, which destabilize the LRS/HRS and consequently lead to large cycle-to-cycle and cell-to-cell variations. In contrast, Kim *et al.* showed that, in a Cu/Ti/AO/TO structure using an AO/TO interfacial 2DEG as the bottom electrode [Fig. 9(d)], the 2DEG provides intrinsic self-compliance that strongly suppresses filament overgrowth and enables highly uniform switching without external current compliance. Here, the key point is not simply that "there is an extra series resistance." As the Cu filament grows and its resistance approaches the 2DEG resistance (e.g., $R_{2DEG} \approx 18\,k\Omega$, $R_{Fila} \approx 40\,K\Omega$, $R_{LRS} \approx 58\,k\Omega$), an increasing fraction of the applied voltages dropped across the 2DEG. By voltage division, the effective potential at the filament tip decreases, so Cu-ion migration and reduction cannot proceed excessively; filament growth becomes self-arrested, stabilizing the SET process. This "built-in" regulation promotes the formation of a small, relatively high-resistance filament near the 2DEG side. Accordingly, Kim *et al.* explained that the SET current is reduced to the $\sim 10\,\mu A$ level, mitigating Joule-heating-driven random rupture, and that RESET tends to be more controllable via ion migration under negative bias. Addressing the counterargument that self-compliance could be achieved simply by adding an external series resistor, Kim *et al.* presented a control experiment in which a device with an external $20\,K\Omega$ series resistor indeed shows self-compliance but fails to RESET. This indicates that the interfacial 2DEG is not an interchangeable lumped resistor; rather, it actively shapes filament morphology and reversibility. Temperature-dependent transport analysis reveals Poole–Frenkel emission at low bias and quantum point contact(QPC)-like conduction after SET, consistent with a thin filament terminated by an atomic-scale tunnel gap. Collectively, Kim *et al.* concluded that the reliability gain in the 2DEG CBRAM stems from limited electron supply at the 2DEG interface and the resulting series voltage division that intrinsically self-limits Cu filament growth, enabling retention longer than 10^6 s at 85 °C and endurance over 10^7 cycles without an external compliance current.[89]

Extending the same "interfacial electron-limited" concept, Kim *et al.* integrated an ALD-grown AO/TO 2DEG bottom electrode into a 3D vertical cell and realized switching via partial filament formation with a finite (maintained) tunnel gap, rather than a fully bridged metallic filament [Fig. 9(e)]. Here, sub-G0 refers to conductance states below the conductance quantum G0 (= 2e2/h, ≈77.5 μS), i.e., a regime in which transport is governed by a partially formed filament terminated by a finite tunnel gap rather than by a fully metallic bridge. In this structure, electrons in the 2DEG are associated with V_O traps

TABLE III. Representative switching metrics of 2DEG-enabled oxide RRAM (CBRAM and OxRAM). This table summarizes key operating and reliability parameters, including forming voltage, SET/RESET voltages, HRS/LRS resistance levels, endurance, retention, and on/off ratio, for reported 2DEG-integrated CBRAM and VCM-type oxide RRAM cells. The listed device stacks provide a concise comparison of switching conditions and memory performance across different material systems and architectures.

	Device	Forming (V)	SET/RESET(V/V)	HRS/LRS(Ω/Ω)	Endurance (cycles)	Retention (s)	On/off ratio
CBRAM	Pt/Cu/Ti/AO/TO[89]	1–5	+1.3/−3	$\sim 10^{10}$–10^{11}/58 $\times 10^3 \sim 10^{10}$	$\geq 10^7$	$>10^6$(@85 °C)	$\sim 10^6$
	Cu/AO/2DEG/W[92]		+4/−4	$\sim 10^6/\sim 10^5$	10^9	∼10	>10
OxRAM	Pt/AO/STO [87]	−4∼−6	−7∼−5/+4.3∼+7	$\sim 10^{10}/\sim 10^4$	10^2		$10^2 \sim 10^3$
	Pt/AO/TO [88]	∼−6	∼−3/∼+3	$10^{11} \sim 10^7/10^5 \sim 10^6$	10^3	10^4(@RT), 10^3(@80 °C)	$\sim 10^4$
	W/2DEG/TO/W[90]	<4	+1/-1	$\sim 3 \times 10^5$ /10^3			$>10^2$

and must be excited before participating in Cu-ion reduction, so the bottom electrode intrinsically limits the electron supply. Therefore, by tuning TO crystallinity to modify 2DEG conductivity (higher crystallinity → higher sheet carrier density and reduced trap depth), the tunnel-gap distance and sub-G_0 conductance can be controlled more deterministically. In addition, Kim *et al.* showed that the tunnel gap can be "tuned" by adjusting the programming voltage, enabling multilevel LRS states. Notably, eight distinct resistance states (3-bit MLC) were achieved in the sub-G_0 regime, and under optimized programming (∼2.5 V), the device exhibits high nonlinearity (∼10^2) with ON/OFF > 10, supporting selector-less crossbar operation. However, because the ON state corresponds to a "partial filament with a finite gap," the LRS can degrade relatively quickly at elevated temperature (e.g., 358 K), limiting long-term retention as a nonvolatile memory. Conversely, because partial-filament switching requires less ionic transport, the pulse endurance exceeds 10^9 cycles and analog conductance updates are highly reproducible. Thus, Kim *et al.* positioned this platform as more suitable for neuromorphic synaptic devices or short-retention memory applications than for long-term nonvolatile storage.[92]

b. OxRAM. 2DEGs have recently been exploited to mitigate the intrinsic variability of OxRAM. In conventional VCM cells, stochastic nucleation/growth of V_O filaments and frequent current overshoot broaden the cycle-to-cycle and cell-to-cell distributions of switching voltages and resistance states. In a 2DEG-enabled strategy, the conductive oxide interface is engineered to function both as the bottom electrode and as a V_O reservoir, enabling more controlled defect exchange with the switching oxide. Moreover, by engineering the V_O concentration/distribution, the switching mode can be intentionally steered from filamentary F-RRAM toward trap-controlled SCLC switching (S-RRAM) or interface-type barrier modulation (I-RRAM), which can substantially improve switching uniformity.[88,91]

In Pt/AO/STO stacks, Miron *et al.* explicitly established what "a V_O reservoir" means in practice: the AO/STO interfacial 2DEG serves as a conductive back electrode whose V_O population can be electrically driven to act as a source/sink for the adjacent insulating AO [Fig. 9(f)]. Under bias, V_Os are injected from (and partially retracted back to) the interface region, so resistive switching is realized inside an initially insulating ALD-AO layer while the defect exchange remains localized near the interface rather than being supplied by a uniformly defect-rich bulk oxide. This reservoir-assisted V_O exchange enables reproducible bipolar operation with a large memory window (HRS > 3.5GΩ and LRS < 10^5Ω, i.e., > 4 decades), and it motivates the broader view that conductive oxide interfaces can "meter" the defect supply that governs VCM switching.[87]

Building on the same reservoir concept but in a technologically scalable materials/process space, Li *et al.* implemented ALD-grown AO/TO conductive-oxide interfaces (and the associated interfacial conduction) on Si-compatible back-end stacks [Fig. 9(g)]. Rather than emphasizing a new filament model, they highlight the practicality of a 2DEG-like conductive interface as a scalable defect reservoir and bottom contact that supports stable bipolar switching and robust resistance windows, verified through an operate-and-verify methodology to demonstrate stability under repeated cycling.[88]

Toward nanoscale integration, Kim *et al.* applied an ALD-derived AO/TO interfacial 2DEG electrode to W/2DEG/TO/W cells scaled from 500 nm down to 30 nm [Fig. 9(h)] and explicitly showed that shrinking the cell area itself shifts the dominant VCM mechanism from interfacial switching to localized filamentary switching. Here, the quoted 30–500 nm dimensions refer to the electrically active switching area, defined by the overlap of the patterned W electrodes, whereas the underlying 2DEG was formed and contacted within a larger micrometer-scale patterned oxide region to enable electrical access. In other words, the 2DEG is not laterally confined to 30 nm in this device; rather, it serves as the bottom electrode/reservoir beneath the nanoscale switching cell, while only the nanoscale overlap region participates directly in resistive switching. In large-area devices (∼500 nm), the reset state can be dominated by area-proportional interfacial transport (e.g., Schottky-type emission through an oxygen-deficient interfacial region), whereas at 30 nm that distributed interfacial current becomes comparatively negligible and conduction localizes into a V_O filament, making filamentary switching dominant. In the 30 nm scaling regime, the interfacial 2DEG contributes both a series-resistance effect and an oxygen-scavenging function that assists V_O formation in TO, which suppresses current overshoot; consequently, the set/reset voltages drop to about ±1 V (from ±2 V without the 2DEG), and the HRS/LRS and set/reset distributions become narrower than those of the W/TO/W control while maintaining ON/OFF > 10^2. Finally, a 1S1R measurement using an NbO_2 IMT selector supports crossbar-array applicability at the 30 nm node.[90]

Finally, Kim *et al.* moved beyond a purely filament-centric narrative by using a vertically formed nanoscale 2DEG (V-2DEG) as both a bottom electrode and a controllable V_O reservoir in W/TO/V-2DEG cells (effective area ≈ 300 nm^2; TO ≈ 5 nm) [Fig. 9(i)], making "mode conversion" the central message. Here, the RTA temperature directly programs the amount and spatial distribution of V_O thermally migrated from the V-2DEG into TO: at moderate annealing (e.g., 300 °C), V_Os are injected into a level that supports distributed trap populations, so the HRS → LRS transition is governed by trap-controlled SCLC rather than stochastic filament formation/rupture, yielding < 1 V bipolar switching with markedly tightened statistics ($\sigma/\mu \approx 0.1$ for both resistances and switching voltages). At higher annealing (e.g., 400 °C), the V_O concentration becomes excessive, strongly modifying the interfacial barrier so the device crosses over to interface-type switching dominated by Schottky barrier modulation (I-RRAM). In other words, the anneal sets the V_O density/distribution that determines whether transport is bulk-limited (SCLC) or interface-limited (Schottky), and the 2DEG electrode functions as a practical "knob" to select not only performance but also the switching physics.[91]

A broader point is that, in most presently reported 2DEG-RRAM demonstrations, the key functional advantage of the 2DEG is not extreme lateral miniaturization of the conductive interface itself, but the way this interface serves as a tunable bottom electrode and defect/ion reservoir for the much smaller active switching region. Accordingly, future practical implementation will require not only continued scaling of the switching cell but also improved lateral patterning and contacting of low-resistance 2DEG electrodes, because the relatively high sheet resistance of many oxide 2DEGs and the difficulty of microfabricating defect-mediated conductive interfaces into thin lines can become limiting at the array level. In this sense, the recent progress from single-crystal systems toward all-ALD amorphous/polycrystalline conductive oxide interfaces is important: it does

not by itself solve lateral scaling, but it substantially improves process scalability, BEOL compatibility, and the design flexibility needed for high-density integration.

C. Neuromorphic device

Neuromorphic hardware aims to process information using device-level dynamics that resemble biological neurons and synapses, enabling efficient temporal computation beyond static weight storage. In particular, liquid state machines (LSMs) exploit rich fading-memory responses in a physical reservoir while keeping training largely at the readout layer.[93] A key hardware challenge is to realize both excitatory and inhibitory (E/I) synaptic behaviors in a compact and controllable form factor, ideally with three-terminal gating that separates state programming from signal readout. Within this context, 2DEG-based oxide memtransistors provide an appealing route because interfacial charge trapping can naturally generate volatile, time-decaying conductance transients suitable for LSM reservoirs and related reservoir computing hardware.[94]

Cheong *et al.* proposed a three terminal neuransistor that integrates a chemically induced 2DEG at the AO/TO_{2-x} interface and exhibits bidirectional short term plasticity, enabling both excitatory postsynaptic potential (EPSP) and inhibitory postsynaptic potential (IPSP) responses within a single device [Fig. 10(a)]. Structurally, while the gate region resembles a conventional 2DEG transistor, in the source/drain region the 2DEG covers the electrodes and effectively acts as a floating electrode, so the overall read current is dominated by the 2DEG/TO_{2-x}/Pt stack rather than by resistance changes in the 2DEG itself. Because both programmed states relax back toward the pristine state (repolarization), the neuransistor naturally exhibits volatile, temporally decaying responses suited to reservoir computing. Importantly, the three-terminal geometry enables in-device masking without complex input preprocessing: an E/I mask routes either EPSP or IPSP-form input to the gate, and an analog regulation-gate mask applied at the source continuously scales the response amplitude. When evaluated as the physical reservoir of a LSM, the neuransistor array delivered substantially improved chaotic time-series prediction compared with an Echo State Network at the same reservoir dimension (e.g., NRMSE ≈ 0.0097 vs 0.1020 on the Hénon map) and reached a given accuracy with roughly threefold fewer training steps.[94]

The relevance of gas sensing to neuromorphic hardware is more naturally understood from the perspective of artificial sensory neurons, especially in olfactory computing. Recent studies on in-sensor neuromorphic noses have shown that a gas sensor can serve not merely as an input transducer but as the receptor-stage element of an artificial olfactory neuron, where the detected chemical stimulus is directly transformed into spike-compatible signals for subsequent SNN processing without bulky intermediate conversion circuitry.[95,96] In this sense, the neuromorphic value of a sensor lies not only in sensitivity itself but in whether its transduction physics can be coupled to temporally encoded neural responses in a compact front-end architecture.

From this standpoint, Kim *et al.* demonstrated an ultrathin H_2 sensor in which the Al_2O_3/TiO_2 interfacial 2DEG serves as a two-dimensional transduction channel while Pd nanoparticles provide catalytic H_2 activation [Fig. 10(b)]. Upon H_2 exposure, Pd forms PdH_x and its work function decreases (≈5.4 eV → ≈4.7 eV), driving electron redistribution across the ultrathin Al_2O_3 and increasing the conductance of the underlying 2DEG; notably, the current change is negligible without Pd, confirming that the Pd–H_2 reaction is essential for modulating the 2DEG channel. Consistent with a 2D electron system that is highly susceptible to surface-induced charge transfer, the sensitivity at 5 ppm improves markedly as the 2DEG sheet density is reduced (from ∼3% at 5.6×10^{13} cm^{-2} up to ∼43% at 4.1×10^{11} cm^{-2}). At room temperature, a device with $ns = 2.7 \times 10^{12}$ cm^{-2} sustains ∼38% sensitivity under repeated 5-ppm cycles and reaches ∼60% at 1% H_2, while a lower-density device ($ns = 1.4 \times 10^{12}$ cm^{-2}) achieves ∼88% sensitivity and maintains reliable detection across a wide 5-ppm–1% concentration range; the response time is $\tau_{90} \approx 28$ s at 5 ppm (recovery time ∼245 s). Importantly, the Al_2O_3 thickness strongly controls the signal transduction: increasing Al_2O_3 from 3 to 7 nm reduces the sensitivity (e.g., ∼15% → ∼2% at 5 ppm), supporting a mechanism in which

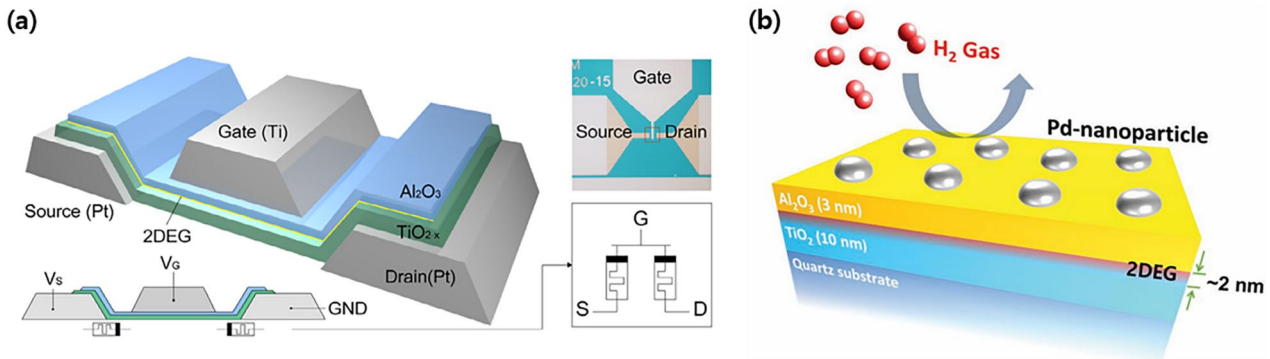

FIG. 10. 2DEG-enabled neuromorphic and sensory device architectures. (a) Schematic of a three-terminal 2DEG neuromorphic transistor ("neuransistor") showing the gate-controlled channel geometry (3D view and cross section) and the corresponding circuit representation. This panel is used to visually define how a single oxide-heterostructure device is configured to implement both excitatory and inhibitory neuronal behaviors via gate modulation of channel conductance. Adapted with permission from W. H. Cheong *et al.*, Adv. Mater. **37**, 2419122 (2025). Copyright 2025 The Authors. Advanced Materials published by Wiley-VCH GmbH. (b) Schematic of a Pd-decorated Al_2O_3/TiO_2 heterostructure hydrogen sensor, where surface H_2 interaction at Pd modulates the transport of the interfacial 2DEG. This panel highlights the "sensory-to-conductance" coupling concept—chemical input (H_2) directly mapped into an electrical output through 2DEG conductivity tuning. Adapted with permission from S. M. Kim *et al.*, Adv. Funct. Mater. **29**, 1807760 (2019). Copyright 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

thicker Al_2O_3 attenuates electron transfer and thus reduces 2DEG modulation. With a total stack thickness below 15 nm, visible-range transmittance of about 83%, and stable operation on polyimide after 500 bending cycles, this 2DEG-based sensor architecture can be understood not only as a high-performance gas sensor but also as a compact sensory transducer whose ultrathin, surface-sensitive channel is well aligned with future artificial olfactory neurons and in-sensor neuromorphic nose platforms.[97]

V. PERSPECTIVES, CHALLENGES, AND FUTURE OUTLOOK

A. General 2DEG perspective

Chemically induced oxide 2DEGs are most usefully understood as process-defined interfacial conduction states whose electronic function is determined by how the interface is formed, confined, and stabilized. Rather than seeking a universally optimal oxide combination, the practical objective is to establish an interfacial state that is suited to the intended device role, for example, as a readily depletable channel, an electrode-like conducting layer, a controllable defect or ion reservoir, or an internal current-limiting element, while remaining sufficiently robust during subsequent integration. For the chemically induced systems emphasized in this review, the most important design variables are the redox conditions during growth, particularly in industry-compatible ALD processes, the transport and trapping characteristics of the adjacent oxide that set the degree of carrier confinement and mobile-carrier fraction, and the stack/passivation design that governs reoxidation, redistribution, and long-term stability.[88] These factors are strongly coupled: increasing interfacial reduction can lower sheet resistance and improve electrode-like behavior, but it can also weaken depletion control, increase leakage, or reduce temporal stability if the surrounding oxide and passivation scheme are not co-optimized. A remaining challenge, however, is that sheet resistance often remains too high for straightforward implementation in many scaled or array-level device concepts.[71] In this sense, future progress will depend not only on improving interfacial conductivity itself but also on developing integration strategies that manage the tradeoff between low sheet resistance, strong confinement, and stable operation under realistic device layouts.

B. 2DEG selector

In ultrathin ALD-AO selector diodes that use conductive-oxide bottom electrodes (Nb:STO or an interfacial 2DEG), performance is often limited less by electrode conductivity than by reverse-bias leakage through the AO barrier, which is governed by trap-assisted conduction and is therefore highly sensitive to the AO defect spectrum and its evolution under bias/oxygen exchange.[72] This reframes "2DEG selectors" as a process-control problem: even with similarly conductive bottom electrodes, rectification and standby current can diverge if AO near-interfacial/border traps differ across wafers or drift over time. A practical mitigation path supported across AO dielectric studies is to (i) tighten the ALD including deposition temperature, precursor dose, and purge conditions that measurably affect near-interfacial trap formation, (ii) use post-deposition oxidation/annealing to reduce V_O-related traps and suppress leakage, and (iii) account explicitly for standard microfabrication steps, since thermal baking, UV exposure, resist processing, and etch/clean sequences can perturb the interfacial defect landscape before the device reaches its final stabilized state. In practice, this means that defect-sensitive oxide selectors are likely to benefit from fabrication flows that place the strongest thermal/UV perturbations before the final defect-conditioning step, followed by a post-patterning stabilization treatment and then encapsulation. Because ambient oxygen/moisture can reconfigure oxide defects and accelerate drift, selector-relevant reliability also benefits from encapsulation/passivation barrier stacks (e.g., AO/SiN_x-type passivation commonly used to improve oxide-electronics environmental stability).[98,99] Finally, the high-impact integration step is to translate the all-oxide concept from single-crystal STO substrates to Si-compatible thin-film conductive-oxide electrodes, while preserving wafer-level control of the AO defect landscape under BEOL thermal budgets.

In 2DEG FETs, one of the clearest opportunities, but also one of the central bottlenecks, is threshold-voltage (V_{th}) control. Compared with conventional Si MOSFETs, oxide 2DEG channels offer a more process-programmable interfacial conduction state, so V_{th} can, in principle, be tuned more directly through growth and post-treatment conditions.[35,40,61] At the same time, however, the inherently high interfacial electron density that makes these channels attractive for conduction also drives V_{th} strongly in the negative direction, making depletion-mode operation a persistent challenge. As a result, V_{th} tuning is not simply an optimization variable but a prerequisite for practical device operation. Existing approaches, such as adjusting the thermal budget, modifying channel thickness or microstructure, or applying electrical conditioning, have indeed shifted V_{th}, but they rarely act on V_{th} alone. Instead, they typically perturb other key performance parameters at the same time, including on-current, mobility, subthreshold slope, hysteresis, and long-term bias stability. For example, lowering the mobile carrier density can improve turn-off characteristics and shift V_{th} positively, but often at the cost of reduced Ion; conversely, improving crystallinity can enhance transport yet also increase the mobile-carrier fraction and push V_{th} back in the negative direction. In this sense, V_{th} control in 2DEG FETs should be viewed as both an opportunity for functional design and a major device-level tradeoff problem. This is also why process-driven V_{th} engineering is already extending beyond device optimization into circuit concepts. Choi *et al.* demonstrated ternary-logic transistors by intentionally generating distinct V_{th} states using multi-stacked 2DEG channels in ultrathin oxide heterostructures, where thickness- and microstructure-dependent carrier control enables multi-level switching beyond binary logic.[100] The remaining challenges are therefore clear: to achieve finer V_{th} control without simultaneously degrading other operating parameters, to maintain long-term V_{th} stability against oxygen exchange and bias-stress drift, and to secure wafer-scale uniformity of the ns–μ–Rsh operating window under BEOL-compatible thermal budgets. Practically, the most transferable mitigation routes include stack-level control of oxygen chemical potential and diffusion using dense encapsulation and diffusion barriers, defect conditioning with BEOL-compatible post-treatments to suppress hysteresis and drift, and closed-loop process control using in-line electrical monitors such as Rsh and V_{th} statistics to keep the programmed interfacial state within a manufacturable window.

C. 2DEG memory

For oxide 2T0C DRAM, the main value of an interfacial 2DEG channel is that it can be driven close to full depletion, so retention is

ultimately limited by leakage in the gate and dielectric stack rather than by channel conduction alone. In stacked implementations, this shows up as a bias window where channel off current and gate leakage trade against each other, and retention improves when V_{th} and dielectric leakage are co engineered by oxide optimization,[101] work function tuning,[102] and dipole approaches.[103] The next step is to reduce or remove the need for global back gate assist by pushing leakage control into the local stack and layout, with dielectric hardening under the 3D thermal budget and interface state control that keeps V_{th} in a usable range without extra biasing.

Ferroelectric memories are a strong match for oxide 2DEGs because an ultrathin, fully depletable interfacial channel keeps C_{dep} small, which improves voltage coupling to the ferroelectric and supports more complete erase in FeFETs while also enabling oxide compatible electrode operation in FRAM stacks. A central constraint is that the oxides used to form or host the 2DEG, such as AO and TO, must not introduce excessive depolarization field or screening that weakens polarization switching. Recent FeFET work provides a practical process lesson: crystallize HZO first, then deposit TO and form the 2DEG afterward, so the 2DEG is not directly exposed to the ferroelectric crystallization step while the channel remains tightly confined and readily depleted. FRAM demonstrations on STO highlight the other end of the spectrum where a conductive interface and ferroelectricity can coexist, but reliance on single crystal substrates and PLD growth limits scalability and integration. A plausible next step is a vacuum continuous ALD route that uses a small number of TMA cycles to establish the conductive interface and then continues directly to HZO deposition followed by crystallization, but this requires an explicit thermal stability check of the 2DEG during the HZO anneal because V_O redistribution and reoxidation can erase the interfacial conductor. For both FeFET and FRAM, monolithic 3D integration will ultimately depend on keeping the ferroelectric, the 2DEG, and adjacent oxides stable under BEOL constraints, which points to controlling oxygen transport with diffusion barriers and oxygen blocking caps, and choosing process sequences that preserve the intended interfacial state after all thermal steps.

For RRAM, an interfacial 2DEG is useful because it can act as an electrode that also moderates filament formation through local oxygen exchange and built in current limiting, which improves switching uniformity in scaled cells and remains compatible with selector integrated operation such as 1S1R demonstrations. In CBRAM type cells, restricting electron supply from V_O trapped carriers provides an additional self-limiting path that can further smooth filament growth. The array level challenge is that the same sheet resistance that helps local regulation can become a line loss penalty if the 2DEG must spread current laterally over long distances. Layout and metallization therefore need to keep the 2DEG path local to each cell, while handing long range routing to low resistance wiring, so the cell keeps the benefits of local regulation without accumulating position dependent write dispersion.

D. 2DEG neuromorphic

Neuromorphic hardware offers a near-term opportunity for oxide 2DEG devices because an interfacial 2DEG can naturally exhibit volatile, history-dependent analog responses that are useful for reservoir computing, without relying on large nonvolatile memory windows or filament formation. In particular, such transient conductance dynamics are well matched to temporal processing frameworks such as liquid state machines, where fading-memory behavior is more important than long-term state retention.[93,94] At the same time, because time-decaying conductance dynamics are also a key ingredient in leaky-integrate-and-fire neuronal operation, these oxide 2DEG devices may also provide a useful materials platform for future spiking neuromorphic hardware.

In the neuransistor, both excitatory and inhibitory short-term plasticity can be obtained in a single device by changing the gate-bias polarity, and the behavior is attributed to charge trapping and detrapping at an ultrathin Al_2O_3/TiO_{2-x} interface that controls the interfacial 2DEG. This points to a practical device role as a hardware time-response element whose fading-memory behavior is set by an engineered trap landscape, matching a key requirement of reservoir-type temporal processing. The main challenge, however, is not simply to demonstrate such dynamics but to make them predictable, reproducible, and compatible with integration. One clear direction is to reduce the operating voltage by improving gate coupling and by choosing thickness and dielectric constant so that the same time-dependent response can be reached at lower electric field. Another direction is reliability control, because the state variable is tied to traps and redox-related defects, so the trap spectrum and interfacial defect state must remain stable under cycling, ambient exposure, and thermal budget. A practical route is therefore to treat the interface as the primary reliability boundary and co-design passivation or oxygen-blocking layers with field-management interlayers so that the time response does not drift beyond what system-level calibration can tolerate. Even so, substantial work is still required to mature this concept into a robust neuromorphic hardware platform.[94]

The ultrathin 2DEG H_2 sensor is a complementary example that is more naturally interpreted in the context of artificial sensory neurons, especially for olfactory neuromorphic systems, where surface chemistry modulates an interfacial electron system through an ultrathin dielectric. In $Pd/Al_2O_3/TiO_2$ sensors, PdH_x formation changes the Pd work function and induces a conductance change in the 2DEG at the Al_2O_3/TiO_2 interface.[97] Because this scheme can be implemented as an ultrathin, transparent, and flexible stack, it supports in-sensor integration rather than only stand-alone sensing. In this sense, its relevance is not merely that it functions as a high-performance H_2 sensor, but that it illustrates how a chemically sensitive oxide 2DEG transducer could serve as the receptor-stage element of an artificial olfactory neuron or neuromorphic nose platform.[95,96] For deployment, the next steps are selectivity and baseline stability, especially against humidity and environment-driven drift, so materials-side stabilization and system-side drift compensation should be developed together.

VI. CONCLUSION

Oxide 2DEG has transitioned from idealized model systems toward chemically programmable electronic interfaces. As reviewed here, a unifying theme across diverse material platforms is that interfacial conduction is governed not only by electrostatics, but critically by V_O generation, redox reactions, and surface chemistry. Among these routes, ALD–enabled V_O formation has emerged as a particularly powerful and scalable pathway, allowing interfacial 2DEG to be created under low-temperature, non-epitaxial, and CMOS-compatible conditions. Importantly, ALD is not only a chemically effective route for 2DEG formation but also a mature and industry-compatible thin-film process, which makes it especially attractive for practical device integration compared with less scalable alternatives.

The maturation of scalable routes, such as ionic bombardment, metal-induced redox, and ligand-driven surface reactions during ALD, has expanded oxide 2DEG into amorphous and polycrystalline stacks beyond conventional perovskite heterostructures. In particular, ALD provides a unique degree of chemical control, where precursor reactivity directly defines interfacial reduction, V_O density, and carrier confinement at the atomic scale. This capability has enabled practical device concepts, including two- and three-terminal selectors, memory elements, and neuromorphic components, where the interfacial 2DEG serves not merely as a conductive layer but as an active, defect-coupled electronic channel. This combination of chemical tunability and process maturity is a key reason why ALD-based oxide 2DEGs are especially promising from a manufacturing perspective.

Despite these advances, key challenges remain. Precise spatial and temporal control of V_O is still limited, and long-term stability under electrical and thermal stress must be better understood, especially for chemically driven interfaces. Moreover, while material-level descriptors such as oxide formation enthalpy and ALD precursor chemistry provide qualitative design rules, a quantitative framework linking interfacial chemistry to device-level performance and variability is still lacking.

Looking forward, oxide 2DEGs should be viewed not as a single materials class but as a general interface-engineering paradigm. Continued progress in ALD-based chemical control of V_O, combined with operando characterization and predictive modeling, will be central to translating oxide 2DEGs into reliable selectors, memory technologies, and neuromorphic hardware, positioning them as a foundational platform for future energy-efficient computing systems.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Seungju Yoon: Conceptualization (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Hyun Jae Lee:** Conceptualization (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Taehwan Moon:** Conceptualization (equal); Funding acquisition (lead); Supervision (lead); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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